DATA SHEET

TDA8000; TDA8000T
Smart card interface

Product specification
Supersedes data of 1995 Feb 01
File under Integrated Circuits, IC02

1996 Dec 12

Philips
Semiconductors

PHILIPS

FEATURES

- Two protected I/O lines
- V_{CC} regulation (5 V ±4%, 100 mA max. with controlled rise and fall times)
- V_{PP} generation (12.5, 15 or 21 V ±2.5%, 50 mA max. programmable by two bits, with controlled rise and fall times)
- Clock generation (up to 8 MHz)
- Short-circuit, thermal and card extraction protections
- Two voltage supervisors (digital and analog supplies)
- Automatic activation and deactivation sequences via an independent internal clock
- Enhanced ESD protections on card connections (4 kV min.)
- ISO 7816 approval.

APPLICATIONS

- Pay TV
- Telematics
- Cashless payment
- Multipurpose card-readers, etc.

GENERAL DESCRIPTION

The TDA8000 is a complete, low-cost analog interface which can be positioned between a smart card or a memory card (ISO 7816) and a microcontroller. It is approved for banking, telecom and pay TV applications.

The complete supply, protection and control functions are realized with only a few external components, which makes the TDA8000 very attractive for consumer applications. Application suggestions and support is available on request (see examples in Chapter “Application information”).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		6.7	–	18	V
I_{DD}	supply current	idle mode; V_{DD} = 12 V	–	25	–	mA
		active modes; unloaded	–	32	–	mA
V_{th2}	threshold voltage on V_{SUP}		4.5	–	4.68	V
V_{CC}	card supply voltage		4.8	5.0	5.2	V
I_{CC}	card supply current		–	–	–100	mA
V_H	high voltage supply for V_{PP}		–	–	30	V
I_{PP}	programming current	read mode; V_{PP} = 5 V	–	–	–50	mA
		write mode; V_{PP} > 5 V	–	–	–50	mA
t_{de}, t_{act}	deactivation/activation cycle duration		–	–	500	µs
P_{tot}	continuous total power dissipation	TDA8000; T_{amb} = +70 °C; see Fig.10	–	–	2	W
		TDA8000T; T_{amb} = +70 °C; see Fig.11	–	–	0.92	W
T_{amb}	operating ambient temperature		0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8000	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA8000T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

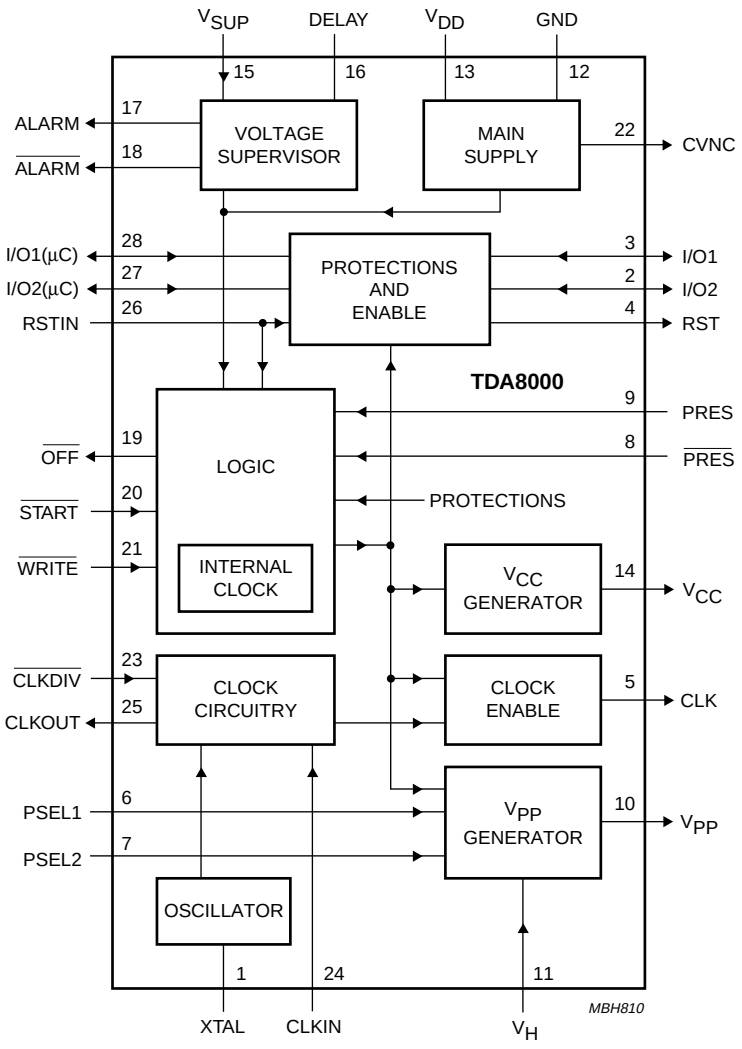


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal connection
I/O2	2	data line to/from the card
I/O1	3	data line to/from the card
RST	4	card reset output
CLK	5	clock output to the card
PSEL1	6	programming voltage selection input (see Table 1)
PSEL2	7	programming voltage selection input (see Table 1)
$\overline{\text{PRES}}$	8	card presence contact input (active LOW)
PRES	9	card presence contact input (active HIGH)
V_{PP}	10	card programming voltage output
V_H	11	high voltage supply for V_{PP} generation
GND	12	ground
V_{DD}	13	positive supply voltage
V_{CC}	14	card supply output voltage
V_{SUP}	15	voltage supervisor input
DELAY	16	external capacitor connection for delayed reset timing
ALARM	17	open-collector reset output for the microcontroller (active HIGH)
$\overline{\text{ALARM}}$	18	open-collector reset output for the microcontroller (active LOW)
$\overline{\text{OFF}}$	19	interrupt output to the microcontroller (active LOW)
$\overline{\text{START}}$	20	microcontroller input for starting session (active LOW)
$\overline{\text{WRITE}}$	21	control input for applying programming voltage to the card (active LOW)
CVNC	22	internally generated 5 V reference, present when V_{DD} is on; to be decoupled externally (47 nF)
$\overline{\text{CLKDIV}}$	23	input for dividing/not dividing the CLKOUT frequency by two (active LOW)
CLKIN	24	external clock signal input
CLKOUT	25	clock output to the microcontroller, or another TDA8000
RSTIN	26	card reset input from the microcontroller (active HIGH)
I/O2(µC)	27	data line to/from the microcontroller; must not be left open-circuit, tie to CVNC if not used
I/O1(µC)	28	data line to/from the microcontroller; must not be left open-circuit, tie to CVNC if not used

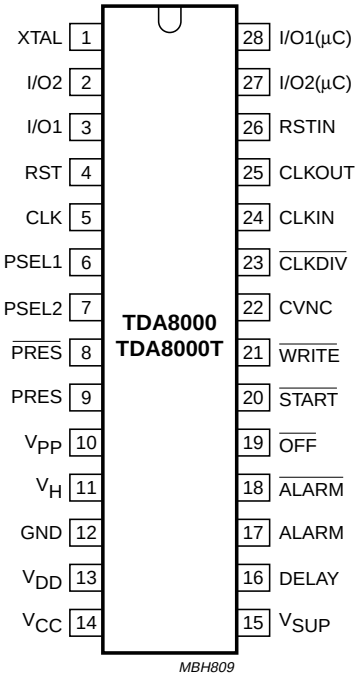


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power supply

The circuit operates within a supply voltage range of 6.7 to 18 V. V_{DD} and GND are the supply pins. All card contacts remain inactive during power-up or power-down, provided V_{DD} does not rise or fall too fast (0.5 V/ms typ.).

POWER-UP

The logic part is powered first and is in the reset condition until V_{DD} reaches V_{th1}. The sequencer is blocked until V_{DD} reaches $V_{th4} + V_{hys4}$.

POWER-DOWN

When V_{DD} falls below V_{th4}, an automatic deactivation of the contacts is performed.

Voltage supervisor

This block surveys the 5 V supply of the microcontroller (V_{SUP}) in order to deliver a defined reset pulse and to avoid any transients on card contacts during power-up or power-down of V_{SUP}.

The voltage supervisor remains active even if V_{DD} is powered-down.

POWER-UP

As long as V_{SUP} is below $V_{th2} + V_{hys2}$ the capacitor C_{DEL}, connected to the pin DELAY, will be discharged. When V_{SUP} rises to the threshold level, C_{DEL} will be recharged. ALARM and $\overline{\text{ALARM}}$ remain active, and the sequencer is blocked until the voltage on the pin DELAY reaches V_{th3}.

POWER-DOWN (see Fig.3)

If V_{SUP} falls below V_{th2}, C_{DEL} will be discharged, ALARM and $\overline{\text{ALARM}}$ become active, and an automatic deactivation of the contacts is performed.

Clock circuitry (see Fig.4)

The clock signal (CLK) can be applied to the card by two different methods:

1. Generation by a crystal oscillator: the crystal (3 to 11 MHz) is connected to pin XTAL. Its frequency is divided by two.
2. Use of a signal frequency already present in the system and connected to the pin CLKIN (up to 8 MHz). Pin XTAL has to be connected to GND via a 1 kΩ resistor. In this event, the CLKOUT signal remains LOW.

In both events the signal is buffered and enabled.

Pin CLKOUT may be used to clock a microcontroller. The signal ($\frac{1}{2}f_{xtal}$ or f_{xtal} if $\overline{\text{CLKDIV}}$ is HIGH) is available when the circuit is powered up.

State diagram

Once activated, the circuit has six possible modes of operation:

- Idle
- Activation
- Read
- Write
- Deactivation
- Fault.

Figure 5 shows how these modes are accessible.

IDLE MODE

After reset, the circuit enters the IDLE state. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- Voltage generators are stopped
- Oscillator is running, providing CLKOUT
- Voltage supervisor is active
- Pins I/O1(μC) and I/O2(μC) are high impedance.

The $\overline{\text{OFF}}$ line is HIGH if a card is present (PRES and $\overline{\text{PRES}}$ active) and LOW if a card is not present.

ACTIVATION SEQUENCE

From the IDLE mode, the circuit enters the ACTIVATION mode when the microcontroller sets the $\overline{\text{START}}$ line (active LOW). The I/O(μC) signals must not be LOW. The internal circuitry is activated, the internal clock starts and the following ISO 7816 sequence is performed:

1. V_{CC} rises from 0 to 5 V
2. I/Os are enabled
3. V_{PP} rises from 0 to 5 V
4. No change
5. CLK is enabled
6. RST is enabled.

The typical time interval between two steps is 32 μs for the first two steps and 64 μs for the other three. Timing is derived from the internal clock (see Fig.6).

Between steps 3 and 5, a HIGH level on pin RSTIN allows the CLK signal to be applied to the card. This feature facilitates a precise count of CLK periods while waiting for the card to respond to a reset.

After step 5, RSTIN has no further action on CLK.

After step 6, RST is set to the complementary value of RSTIN.

READ MODE

When the activation sequence is completed and, after the card has replied to its Answer-to-Reset, theTDA8000 enters the READ mode. Data is exchanged between the card and the microcontroller via the I/O lines.

When it is required to write to the internal memory of the card, the circuit is set to the WRITE mode by the microcontroller.

Cards with EPROM memory require a programming voltage (V_{PP}).

V_{PP} GENERATION

The circuit supports cards with V_{PP} of 12.5, 15 or 21 V. The selection of P is achieved by PSEL1 and PSEL2 according to Table 1.

Table 1 Card programming voltage selection

PSEL1	PSEL2	PROGRAMMING VOLTAGE P
LOW	LOW	5
LOW	HIGH	12.5
HIGH	LOW	15
HIGH	HIGH	21

In order to respect the ISO7816 slopes, the circuit generates V_{PP} by charging and discharging an internal capacitor. The voltage on this capacitor is then amplified by a power stage gain of 5, powered via an external supply pin V_H [30 V (max.)].

WRITE MODE (see Fig.7)

When the microcontroller sets the $\overline{\text{WRITE}}$ line (active LOW), the circuit enters the WRITE mode. V_{PP} rises from 5 V to the selected value with a typical slew rate of 1 V/µs. When the write operation is completed, the microcontroller returns the $\overline{\text{WRITE}}$ line to its HIGH state, and V_{PP} falls back to 5 V with the same slew rate.

$\overline{\text{WRITE}}$ has no action outside a session.

DEACTIVATION SEQUENCE (see Fig.8)

When the session is completed, the microcontroller sets the $\overline{\text{START}}$ line to its HIGH state.

The circuit then executes an automatic deactivation sequence by counting back the sequencer:

1. Card reset (RST falls to LOW)
2. CLK is stopped
3. No change
4. V_{PP} falls to 0 V
5. I/O1(µC) and I/O2(µC) become high impedance
6. V_{CC} falls to 0 V.

The circuit returns to the IDLE mode on the next rising edge of the sequencer clock.

PROTECTIONS

Main fault conditions are monitored by the circuit:

- Short-circuit on V_{CC}
- Short-circuit on V_{PP}
- Over current on I/Os
- Card extraction during transaction
- Overheating problem.

When one of these fault conditions is detected, the circuit pulls the interrupt line $\overline{\text{OFF}}$ to its active LOW state and returns to the FAULT mode.

FAULT MODE (see Fig.9)

When a fault condition is written to the microcontroller via the $\overline{\text{OFF}}$ line, the circuit initiates a deactivation sequence.

After the deactivation sequence has been completed, the $\overline{\text{OFF}}$ line is reset to its HIGH state when the microcontroller has reset the $\overline{\text{START}}$ line HIGH, except if the fault condition was due to a card extraction.

Note

The two other causes of emergency deactivation (Power failure detected on V_{DD} or V_{SUP}) do not act upon $\overline{\text{OFF}}$.

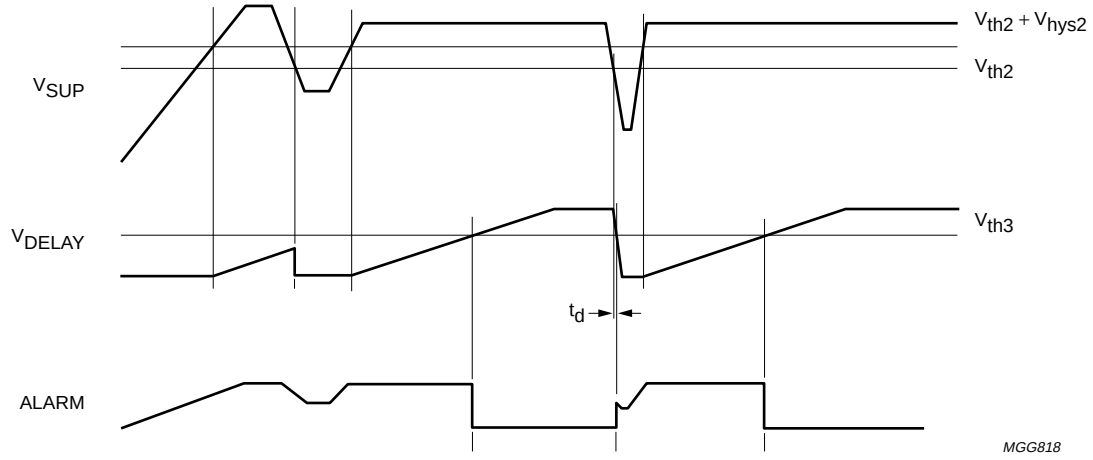


Fig.3 ALARM and DELAY as a function of V_{SUP} (C_{DEL} fixes the pulse width).

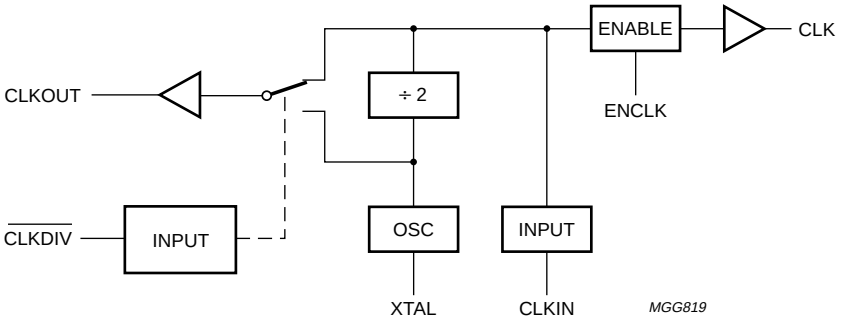


Fig.4 Clock circuitry.

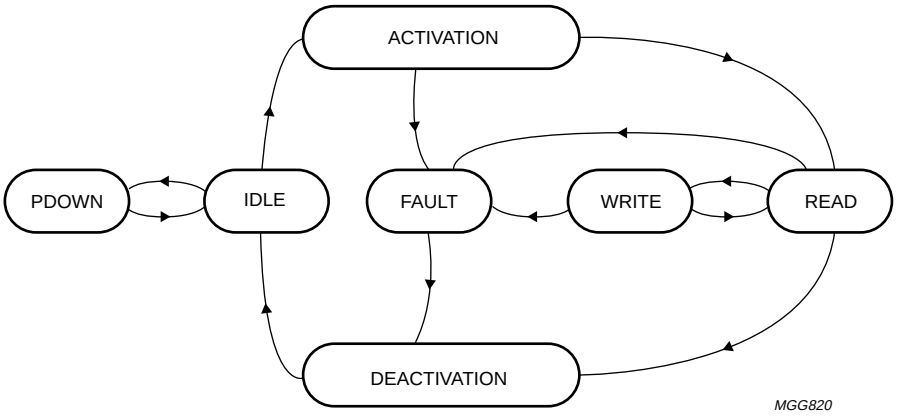


Fig.5 State diagram.

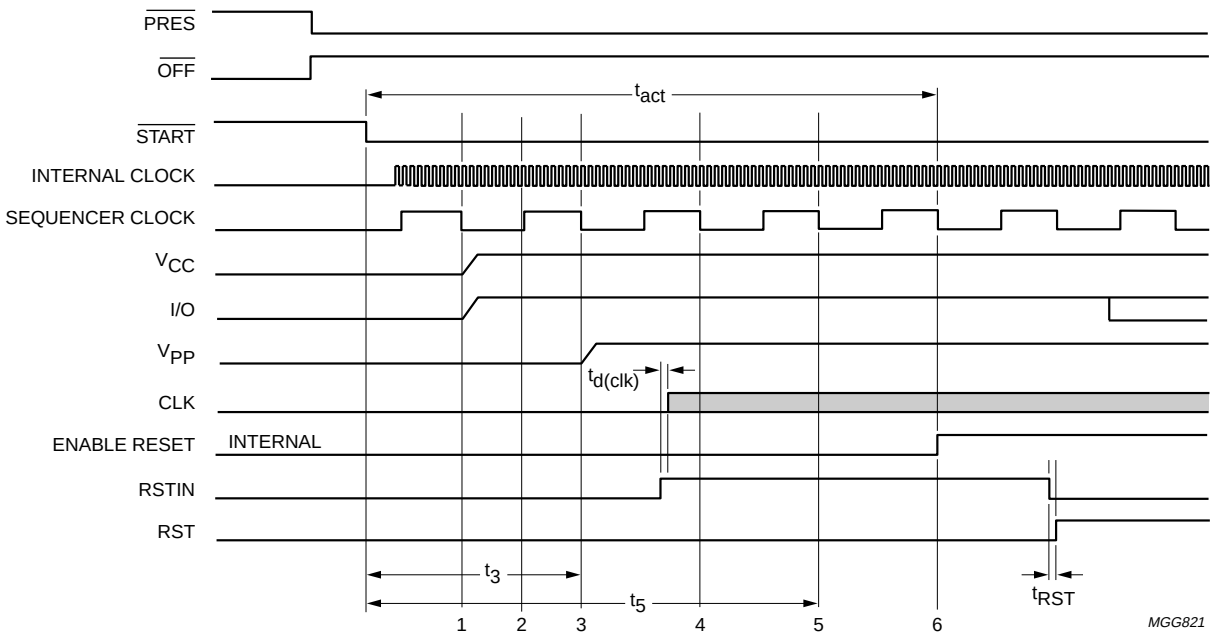


Fig.6 Activation sequence.

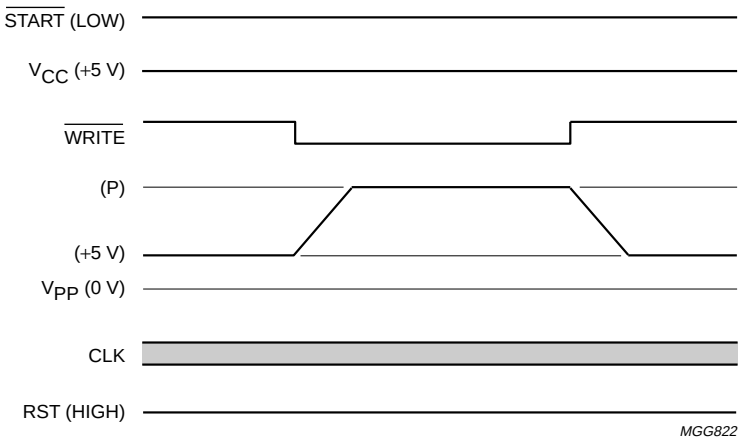


Fig.7 Read/Write; Read mode.

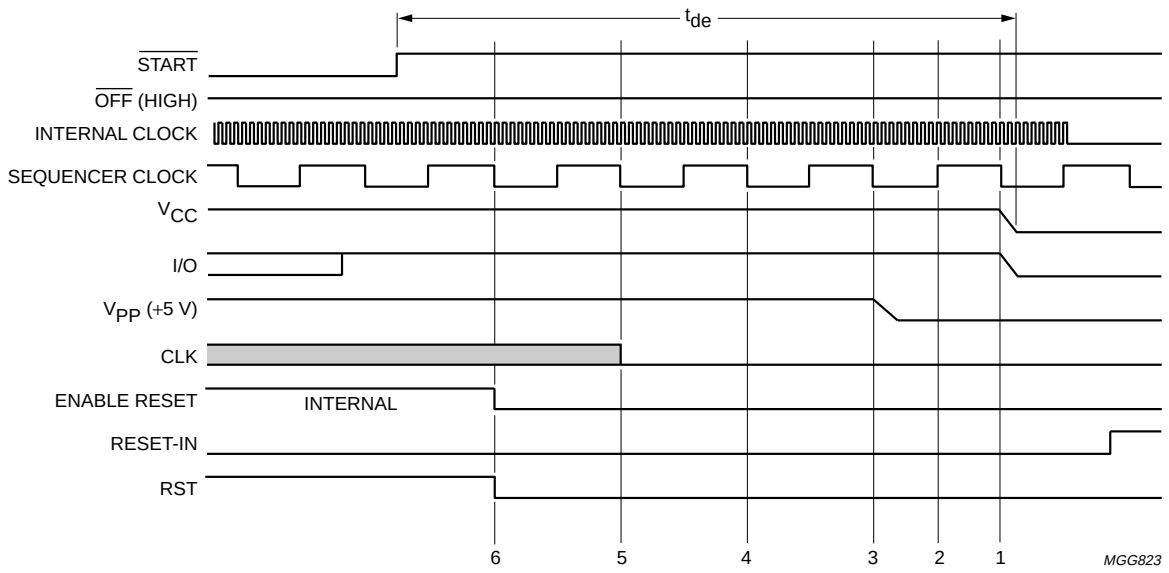


Fig.8 Deactivation sequence after a normal session.

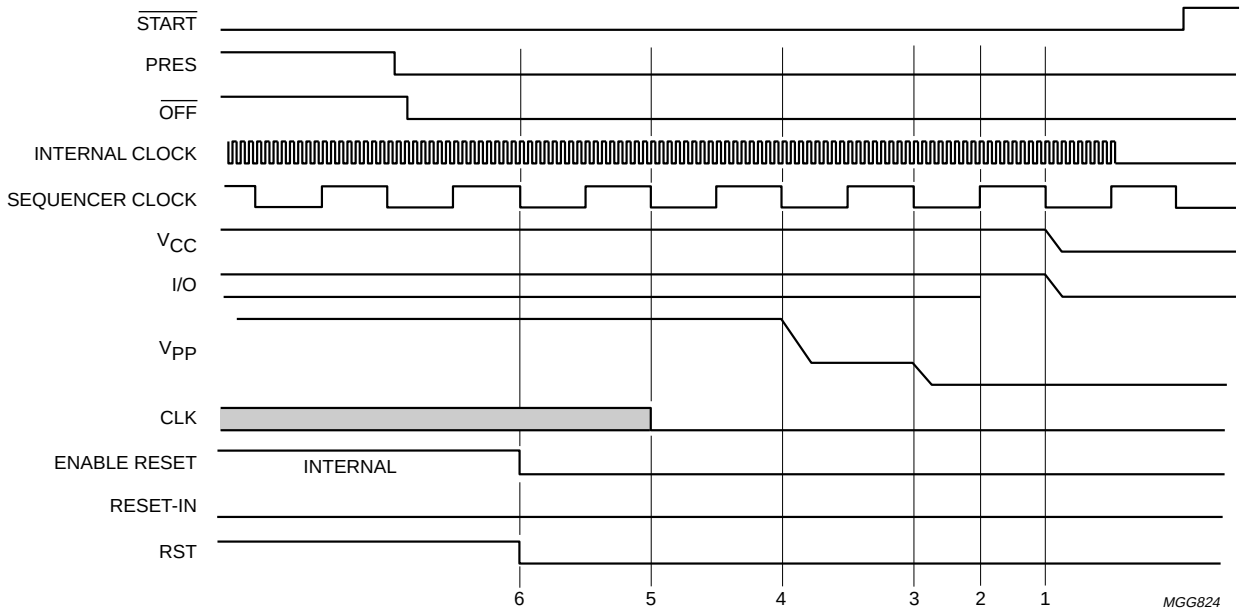


Fig.9 Deactivation after a card extraction during write mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	+18	V
V_{x1}	voltage on pins PSEL1, PSEL2, PRES, $\overline{PRES}$, $\overline{WRITE}$, $\overline{START}$, $\overline{OFF}$, $\overline{ALARM}$ and RSTIN		–0.3	V_{DD}	V
V_H	voltage on pin V_H		–0.3	+30	V
V_{PP}	voltage on pin V_{PP}		–0.3	V_H	V
V_{SUP}	voltage on pin V_{SUP}		–0.3	+12	V
V_{x2}	voltage on pins ALARM and DELAY		–0.3	V_{SUP}	V
V_{x3}	voltage on pins XTAL, I/O1(µC), I/O2(µC), CLKIN, CLKOUT, $\overline{CLKDIV}$ and CVNC		–0.3	+6.0	V
V_{x4}	voltage on pins I/O1, I/O2, RST, CLK and V_{CC}	duration < 1 ms	–0.3	+7.0	V
P_{tot}	continuous total power dissipation	TDA8000; T_{amb} = +70 °C; note 1; see Fig.10	–	2	W
		TDA8000T; T_{amb} = +70 °C; note 1; see Fig.11	–	0.92	W
T_{stg}	storage temperature		–55	+150	°C
V_{es}	electrostatic voltage on pins I/O1, I/O2, V_{CC}, V_{PP}, RST and CLK		–4	+4	kV
	electrostatic voltage on other pins		–2	+2	kV

Note

1. $P_{tot} = V_{DD} \times (I_{DD(unloaded)} + \Sigma I_{signals}) + I_{CC} \times (V_{DD} - V_{CC}) + \max.\{(V_H - V_{PP}) \times I_{PP(read)} + (V_H - V_{PP}) \times I_{PP(write)}\} + V_H \times I_{H(unloaded)} + V_{SUP} \times I_{SUP} + (V_{DD} - CVNC) \times I_{CVNC}$.
   Where ‘signals’ means all signal pins used, excluding the supply pins.

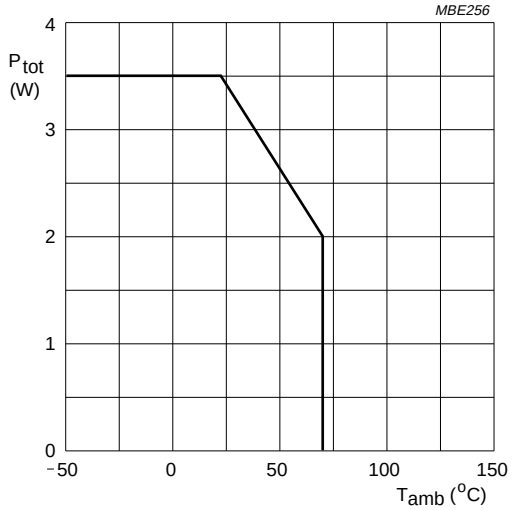


Fig.10 Power derating curve (DIP28).

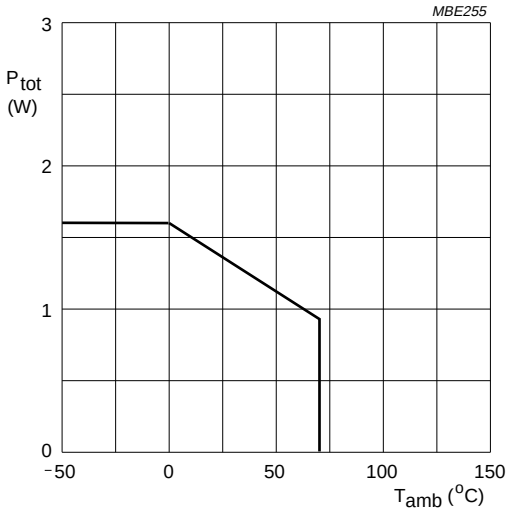


Fig.11 Power derating curve (SO28).

HANDLING

Each pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses positive and 3 pulses negative; on each pin referenced to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	30	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

V_{DD} = 12 V; V_H = 25 V; V_{SUP} = 5 V; f_{xtal} = 7.16 MHz or f_{CLKIN} = 3.58 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		6.7	–	18	V
I_{DD}	supply current	idle mode; V_{DD} = 8 V	16	22	30	mA
		idle mode; V_{DD} = 18 V	20	28	36	mA
		active mode; unloaded	26	32	38	mA
V_{th1}	threshold voltage for power-on reset		1.5	3.0	4.0	V
V_{th4}	threshold voltage on V_{DD} (falling)		6.0	–	6.5	V
V_{hys4}	hysteresis on V_{th4}		50	–	200	mV
Voltage supervisor						
V_{SUP}	supply voltage for the supervisor		–	5	–	V
I_{SUP}	input current on V_{SUP}		–	1.6	2	mA
V_{th2}	threshold voltage on V_{SUP} (falling)		4.5	–	4.68	V
V_{hys2}	hysteresis on V_{th2}		10	–	80	mV
V_{th3}	threshold voltage on DELAY		2.35	–	2.65	V
I_{DEL}	output current on DELAY	pin grounded (charge)	–4	–	–2.5	µA
		V_{DEL} = 4 V (discharge)	6	–	–	mA
V_{DEL}	voltage on pin DELAY		–	–	3.5	V
ALARM, $\overline{\text{ALARM}}$ (open-collector outputs)						
I_{OH}	HIGH level output current on pin $\overline{\text{ALARM}}$	V_{OH} = 5 V	–	–	25	µA
V_{OL}	LOW level output voltage on pin $\overline{\text{ALARM}}$	I_{OL} = 2 mA	–	–	0.4	V
I_{OL}	LOW level output current on pin ALARM	V_{OL} = 0 V	–	–	–25	µA
V_{OH}	HIGH level output voltage on pin ALARM	I_{OH} = –2 mA	V_{SUP} – 1	–	–	V
t_d	delay between V_{SUP} and ALARM	C_{DEL} = 47 nF; see Fig.3	–	–	10	µs
t_{pulse}	ALARM pulse width	C_{DEL} = 47 nF	30	–	65	ms
Interrupt line $\overline{\text{OFF}}$ (open-collector)						
I_{OH}	HIGH level output current	V_{OH} = 5 V	–	–	25	µA
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V
Logic inputs (RSTIN, $\overline{\text{START}}$, $\overline{\text{WRITE}}$, $\overline{\text{CLKDIV}}$, PSEL1, PSEL2, PRES, $\overline{\text{PRES}}$); note 1						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		1.5	–	–	V
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	–20	µA
I_{IH}	HIGH level input current	V_{IH} = 5 V	–	–	20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset output to the card (RST)						
V_{IDLE}	output voltage in IDLE mode		–	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = 200 μA	–	–	0.45	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	4.0	–	V_{CC}	V
		I_{OH} = −10 μA	V_{CC} − 0.7	–	V_{CC}	V
t_{RST}	delay between RSTIN and RST	RST enabled; see Fig.6	–	–	2	μs
t_r	rise time	C_L = 330 pF	–	–	1	μs
t_f	fall time	C_L = 330 pF	–	–	1	μs
Clock output to card (CLK)						
V_{IDLE}	output voltage in IDLE mode		–	–	0.4	V
V_{OL}	LOW level output voltage	I_{OL} = 200 μA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −200 μA	2.4	–	V_{CC} + 0.3	V
		I_{OH} = −20 μA	$0.7V_{CC}$	–	V_{CC} + 0.3	V
		I_{OH} = −10 μA	V_{CC} − 0.7	–	V_{CC} + 0.3	V
t_r	rise time	C_L = 30 pF; note 2	–	–	18	ns
t_f	fall time	C_L = 30 pF; note 2	–	–	18	ns
δ	duty factor	C_L = 30 pF; (XTAL or CLKIN used); note 2	45	–	55	%
$\Delta\delta/\Delta\theta$	thermal drift on duty factor	DIP and SO packages	–	−0.07	–	%/K
Card programming voltage (V_{PP})						
P	selected voltage	see Table 1				
V_{PP}	output voltage	idle mode	–	–	0.4	V
		read mode	V_{CC} − 4%	–	V_{CC} + 4%	V
		write mode; I_{PP} < 50 mA	P − 2.5%[3]	–	P + 2.5%[3]	V
I_{PP}	output current	read mode	–	–	−50	mA
		write mode	–	–	−50	mA
		write mode; V_{PP} short-circuited to GND	–	–	−400	mA
SR	slew rate	up or down	0.80	1.0	1.20	V/μs
High-voltage input (V_H)						
V_H	input voltage		–	–	30	V
I_H	input current at V_H	idle mode	2	–	3	mA
		active mode; unloaded; $\overline{WRITE}$ = 0				
		P = 5 V	3	–	7	mA
		P = 12.5 V	5	–	10	mA
		P = 15 V	6	–	11	mA
		P = 21 V	8	–	13	mA
$V_H - V_{PP}$	voltage drop		–	–	2.2	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card supply voltage (V_{CC})						
V_{CC}	output voltage	idle mode	–	–	0.4	V
		active mode; I_{CC} < 100 mA	4.80	–	5.20	V
I_{CC}	output current		–	–	–100	mA
		V_{CC} connected to GND	–	–	–400	mA
SR	slew rate	up or down	0.80	1.0	1.20	V/µs
5 V reference output (CVNC)						
V_{CVNC}	output voltage at CVNC	I_{CVNC} < –15 mA	4.5	5.0	5.5	V
Crystal connection (XTAL)						
$R_{xtal(neg)}$	negative resistance at crystal	3 MHz < f_i < 11 MHz; note 4	–	–	–300	Ω
V_{xtal}	DC voltage at crystal		3	–	4	V
f_{xtal}	crystal resonant frequency		3	–	11	MHz
External clock input (CLKIN)						
f_{ext}	frequency at CLKIN	note 2	0	–	8	MHz
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		1.5	–	5	V
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	–20	µA
I_{IH}	HIGH level input current	V_{IH} = 2 V	–	–	20	µA
C_I	input capacitance		–	–	5	pF
Clock output (CLKOUT)						
f_{CLKOUT}	frequency on CLKOUT		1	–	8	MHz
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	V_{OH} = –200 µA	3	–	–	V
		V_{OH} = –10 µA	4	–	–	V
t_r, t_f	rise and fall times	C_L = 30 pF; note 2	–	–	25	ns
δ	duty factor	$\overline{CLKDIV}$ = 0; C_L = 30 pF; note 2	45	–	55	%
		$\overline{CLKDIV}$ = 1; C_L = 30 pF; note 2	40	–	60	%
Δδ/Δθ	thermal drift on duty factor	DIP and SO packages	–	–0.1	–	%/C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data lines [I/O1, I/O2, I/O1(μC), I/O2(μC)]; note 5						
V_{OH}	HIGH level output voltage on I/O	$4.5 < V_{SUP} < 5.5$; $4.5 < V_{I/O(\mu C)} < 5.5$; $I_{OH} = -20$ μA	4	–	V_{CC} + 0.2	V
		$4.5 < V_{SUP} < 5.5$; $4.5 < V_{I/O(\mu C)} < 5.5$; $I_{OH} = -200$ μA	2.4	–	–	V
V_{OL}	LOW level output voltage on I/O	$I_{I/O}$ = 1 mA; I/O(μC) grounded	–	–	65	mV
I_{IL}	LOW level input current on I/O(μC)	I/O(μC) grounded; $I_{I/O} = 0$	–	–	–500	μA
		I/O(μC) grounded; I/O connected to V_{CC}	–	–	–5	mA
V_{OH}	HIGH level output voltage on I/O(μC)	$4.5 < V_{I/O} < 5.5$	4	–	V_{SUP} + 0.2	V
V_{OL}	LOW level output voltage on I/O(μC)	$I_{I/O(\mu C)}$ = 1 mA; I/O grounded	–	–	70	mV
I_{IL}	LOW level input current on I/O	I/O grounded; $I_{I/O(\mu C)} = 0$	–	–	–500	μA
		I/O grounded; I/O(μC) connected to V_{SUP}	–	–	–5	mA
V_{IDLE}	voltage on I/O outside a session		–	–	0.4	V
Z_{IDLE}	impedance on I/O(μC) outside a session		10	–	–	MΩ
R_{pu}	internal pull-up resistance between I/O and V_{CC}		17	20	23	kΩ
t_r, t_f	rise and fall times	$C_i = C_o$ = 30 pF	–	–	1	μs
Protections						
T_{sd}	shut-down local temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–175	–	–230	mA
$I_{PP(sd)}$	shut-down current at V_{PP}		–90	–	–140	mA
$I_{I/O(sd)}$	shut-down current at I/O	from I/O to I/O(μC)	3	–	5	mA
Timing						
t_{act}	activation sequence duration	see Fig.6	250	–	500	μs
t_{de}	deactivation sequence duration	see Fig.8	250	–	500	μs
t_3	start of the window for sending CLK to the card	see Fig.6	–	–	140	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_5	end of the window for sending CLK to the card	see Fig.6	160	–	–	µs
t_{st}	maximum pulse width on START before V_{CC} starts rising		–	–	30	µs
$t_{d(clk)}$	delay between RSTIN and CLK	see Fig.6	–	–	2	µs

Notes

1. $\overline{\text{START}}$, $\overline{\text{WRITE}}$, $\overline{\text{CLKDIV}}$ and $\overline{\text{PRES}}$ are active LOW; RSTIN and PRES are active HIGH.
2. The transition time and duty factor definitions are shown in Fig.12; $\delta = \frac{t_1}{t_1 + t_2}$.
3. P is the card programming voltage set by pins PSEL1 and PSEL2.
4. This condition ensures correct start-up of the oscillator with crystals having series resistance up to 100 Ω.
5. The path between I/O and I/O(µC) is as follows (see Fig.13):
   a) Clamp to V_{CC}.
   b) 20 kΩ pull-up resistor to V_{CC}; thus V_{OH} on I/O.
   c) Two opposite npn transistors with sensing pnp transistor.
   d) Clamp to V_{SUP}; thus V_{OH} on I/O(µC).
   e) The base current of the npn transistor is decreasing when their collector current increases. This means the voltage drop is very low for small currents and becomes maximum for some mA. Thus V_{OL} on I/O and I/O(µC), current limits, and high impedance feature. The output current from I/O and I/O(µC) when the line is open-circuit is the sum of the pull-up current and the base currents.

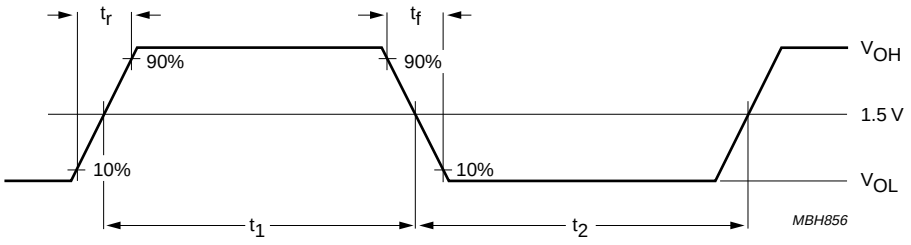


Fig.12 Definition of transition times.

INTERNAL PIN CONFIGURATION

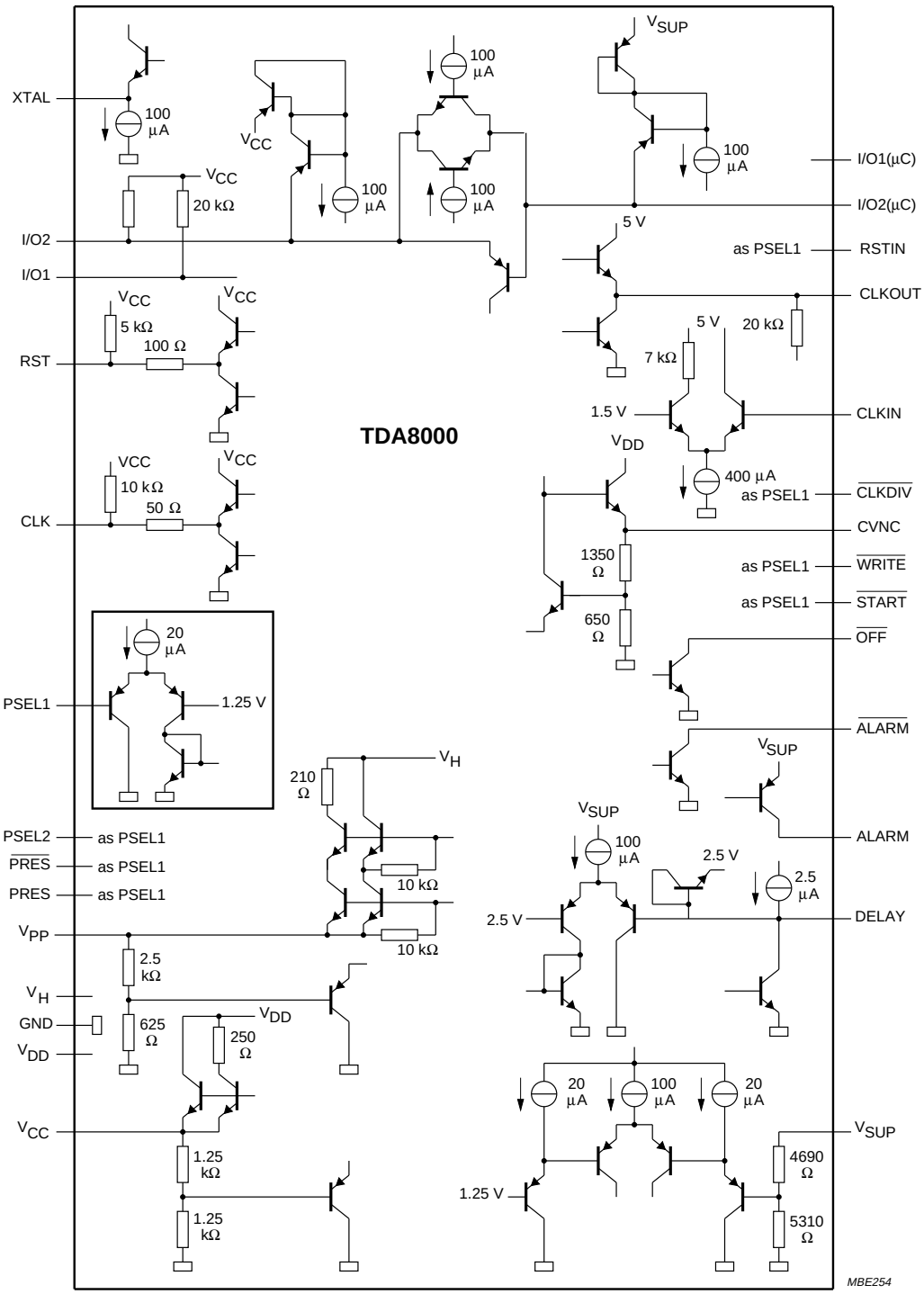


Fig.13 Internal pin configuration.

APPLICATION INFORMATION

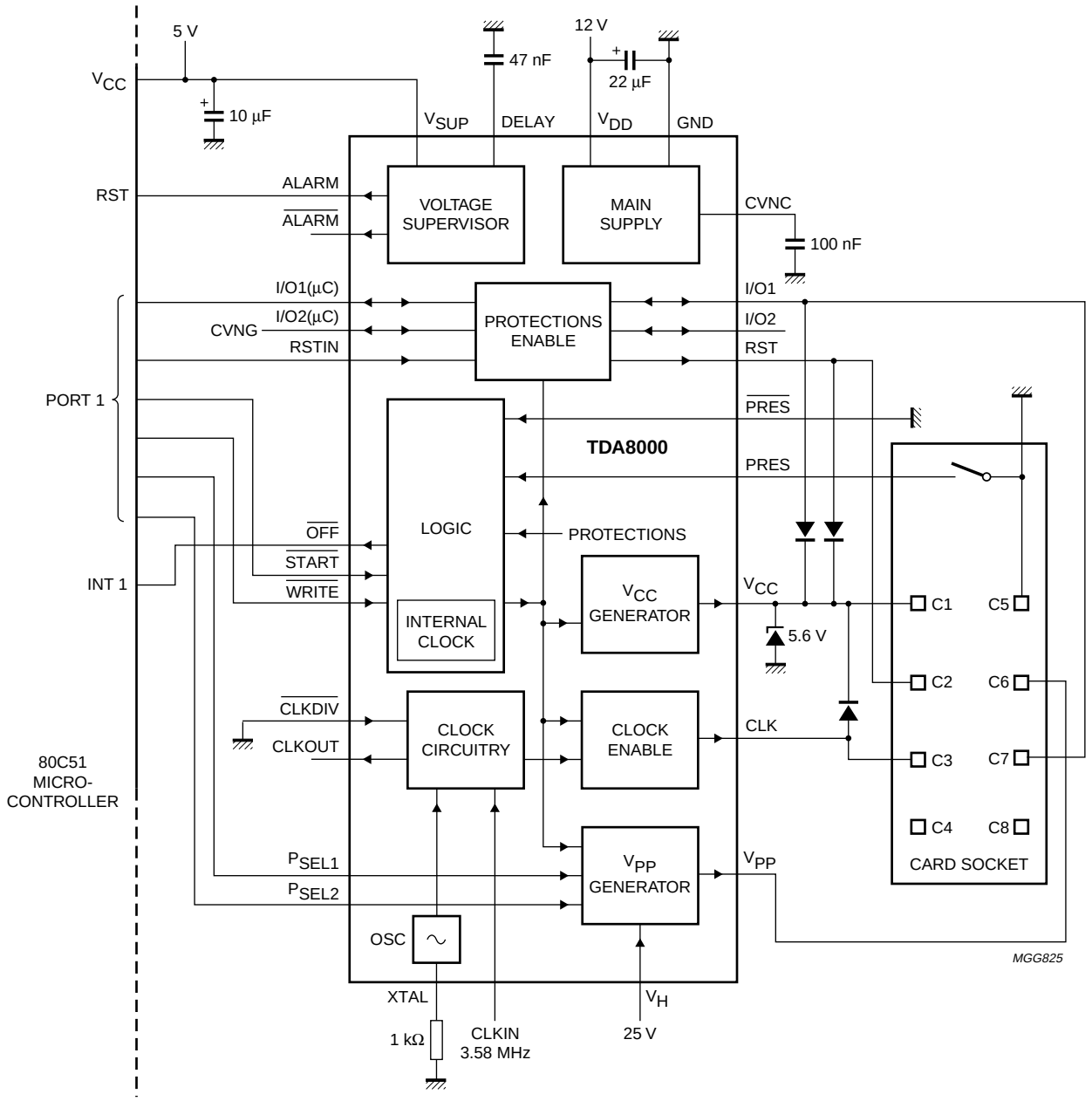
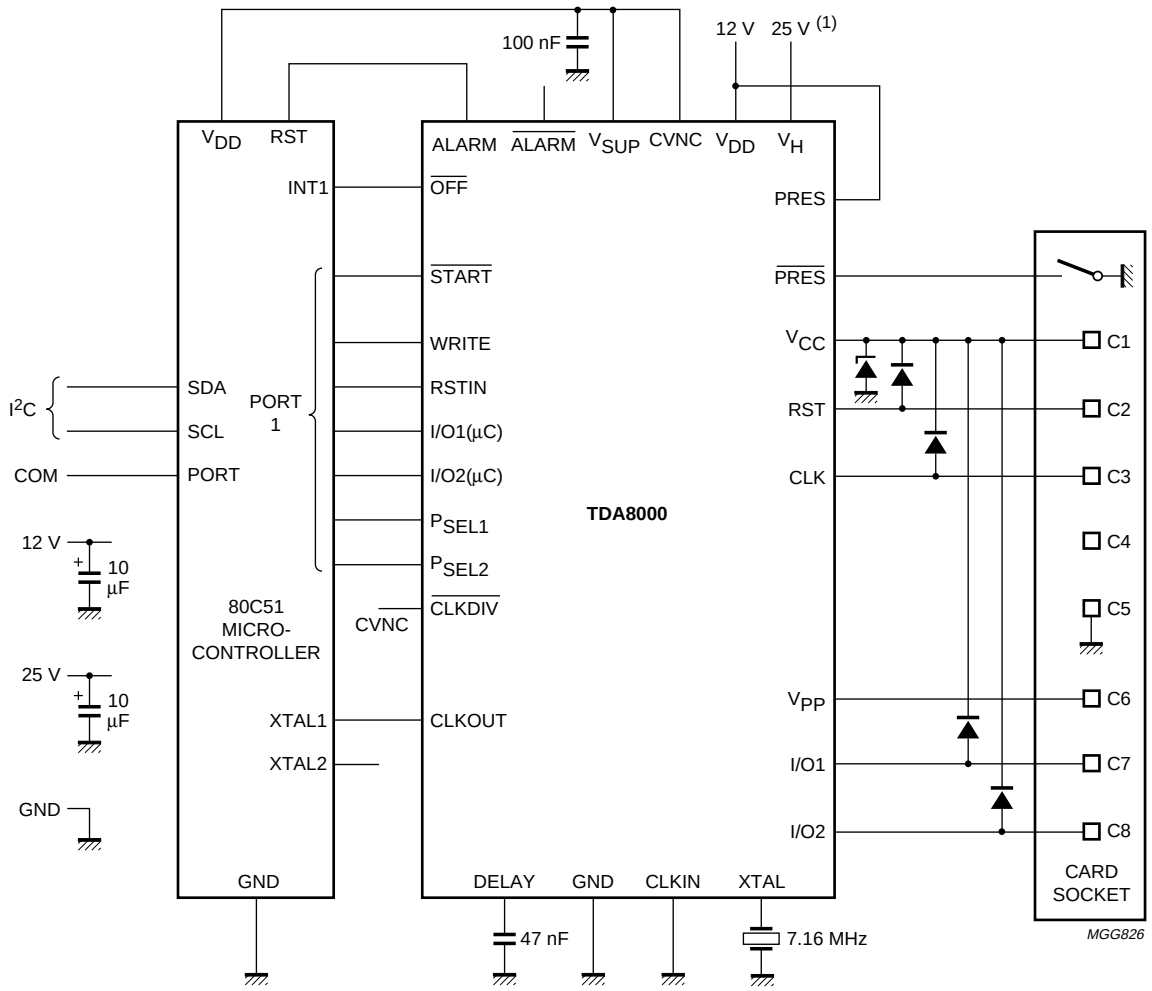


Fig.14 Typical application within a consumer product.

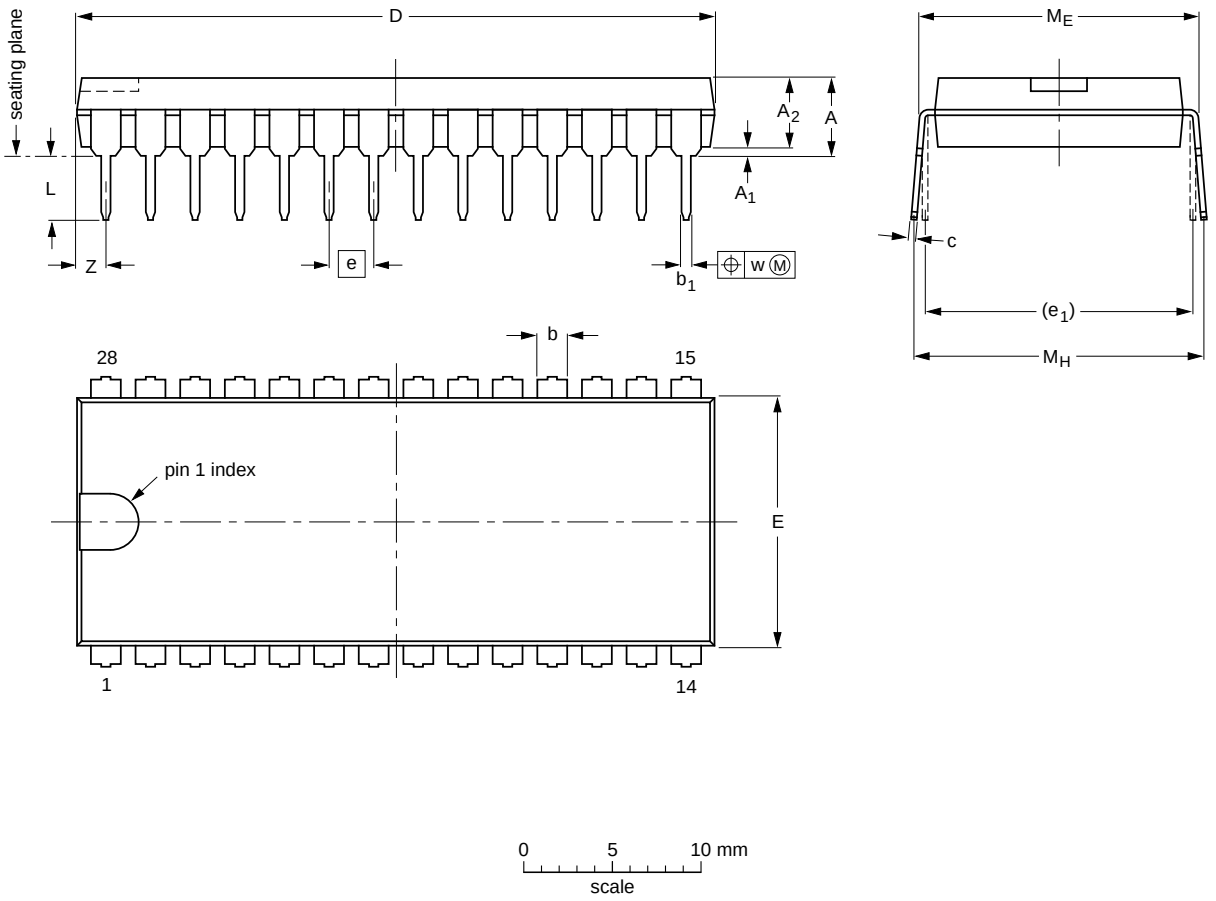


(1) If pin V_H is not connected to 25 V, it should be connected to V_{DD}.

Fig.15 Application in a remote card reader; the microcontroller is clocked and powered by the TDA8000 interface is achieved via the I^2C-bus.

PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

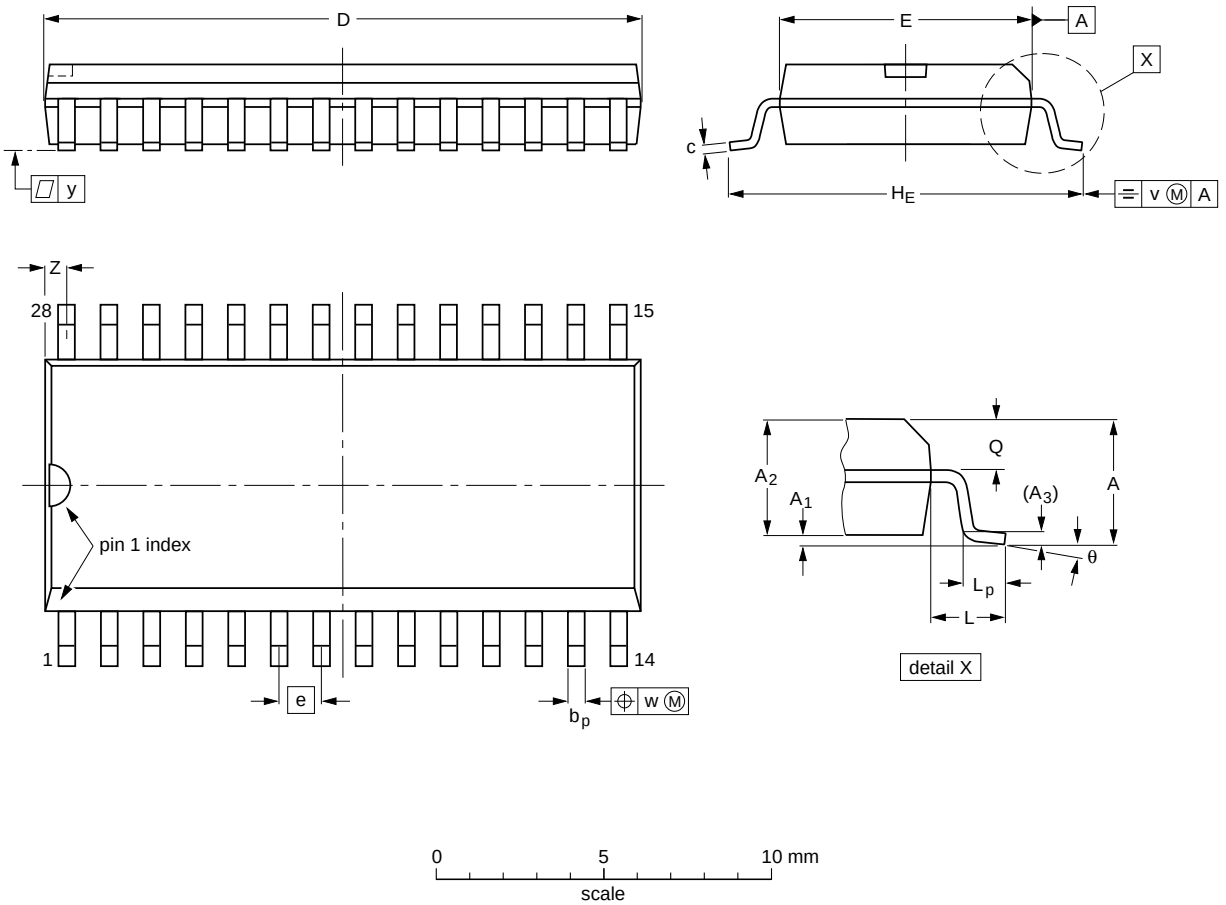
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 537021/1200/04/pp24 Date of release: 1996 Dec 12 Document order number: 9397 750 01383

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