AN-717
Application Note

BATTERY-POWERED 5-MHz FREQUENCY COUNTER

Prepared By
Don Aldridge
Applications Engineering

This application note describes a battery-powered 5-MHz frequency counter using the McMOS logic family for low-power operation. The basic counter is optimized at a 12-volt supply for maximum performance with a linear input-signal conditioner. Several options are discussed which optimize the basic counter for minimum power dissipation. These options include a CMOS input signal-conditioner and multiplexed LED displays.

MOTOROLA *Semiconductor Products Inc.*

BATTERY-POWERED 5-MHz FREQUENCY COUNTER

INTRODUCTION

The current trend in electronic instruments is toward portable operation which requires smaller size, less weight and less power consumption. This application note describes a frequency counter which is designed using low powered logic for portable operation. The power requirements of the counter logic portion is in the order of milliwatts, however, the major portion of the power dissipation is associated with the digital readout display. Therefore, with no input signal present, display blanking has been used to reduce display power consumption.

The counter features:

1) 5 MHz frequency operation.
2) Low powered CMOS logic.
3) Choice of either CMOS or linear front end.
4) Variable time base from 10 seconds to 10 μs.

This note describes the operation of a basic frequency counter followed by a description of the circuit of the basic 5 MHz frequency counter. Included is a section on signal conditioning for frequency counters and a description of a 10 MHz linear front end for the basic counter. This front end was designed for maximum frequency and sensitivity. A second counter is also described that minimizes the power drain considering tradeoffs of frequency, performance, and sensitivity. This counter uses a unique method of decoder multiplexing for the displays and a CMOS front end for signal conditioning.

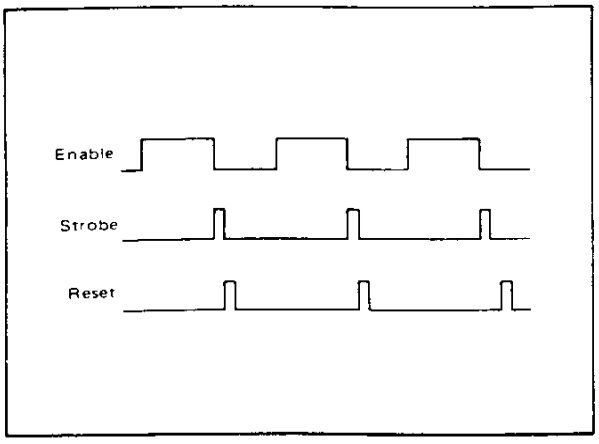

FIGURE 1 – COUNTER FUNCTIONS

BASIC COUNTER OPERATION

The basic function of a frequency counter is to count the number of events per unit time. The electronic frequency counter monitors the input events as transitions between two voltage levels. The actual counting operation takes place during a precise time period called the gating or enable period. This time period is usually generated by a crystal oscillator and a series of decade dividers to produce the desired time period. Enable time length may be changed by selecting the number of decade dividers.

Input voltage transitions are counted by a series of decade counters. The input signal frequency is determined by the number of times the counters have been toggled during the enable time.

The counting sequence consists of three steps:

1. Enable or gating time
2. Strobing the count into latches.
3. Resetting of counters.

Waveforms of this sequence are shown in Figure 1. A block diagram of a basic frequency counter is shown in Figure 2. The sequence is started with the enable pulse which allows the counters to count. At the end of the enable pulse, the output of the counters is strobed or transferred into the latches and displayed on the digital readouts (R/O). After this step is completed the counters are reset and the cycle is ready to repeat. The count is held by the latches while the counters are reset and the sequence is repeated.

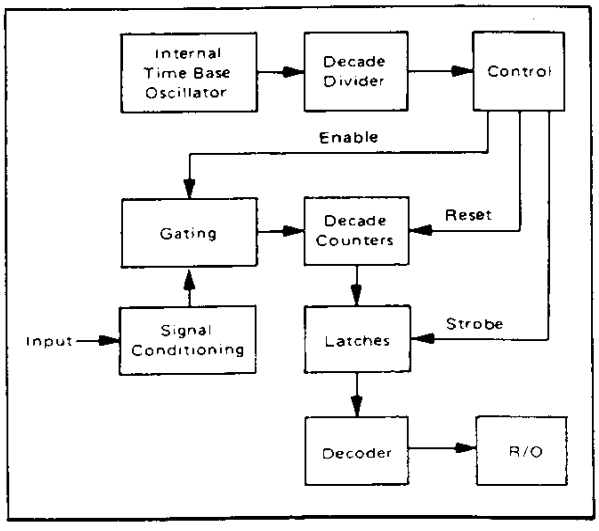

FIGURE 2 – FREQUENCY COUNTER BLOCK DIAGRAM

5 MHz FREQUENCY COUNTER

Motorola's McMOS logic was used to implement the counter logic. The schematic of the counter is shown in Figure 3 and is presented in three basic parts:

1. Crystal oscillator and time base.
2. Counter, latches, decoders and displays.
3. Control functions.

CRYSTAL OSCILLATOR AND TIME BASE

The time base circuitry determines the length of the enable time. The reference frequency is obtained from a 1 MHz crystal oscillator using a CMOS gate, G1, with a crystal as a feedback element. Gate G2 is used as a buffer for the 1 MHz oscillator. Provision for an external reference frequency is provided by switch S1. The external reference must have a 0-10 volt swing to drive the time base counters. This may be used when a more stable reference than the internal oscillator is required. The time base divides the 1 MHz oscillator frequency down to the desired enable time by using MC14518 dual decade counters. Three and one-half dual counters (seven decades) are used to provide a maximum enable period of 10 seconds. The counters are connected in a conventional ripple-through configuration. This type of counter operation has the advantage of simplicity but the disadvantage of a time delay from the input of the first counter to the output of the last counter. This time delay is compensated by the counter control section described later.

COUNTERS, LATCHES, DECODERS AND DISPLAYS

The MC14518 dual BCD counter is used for the actual counting of the input signal. Although the CMOS logic family is capable of operation over a wide voltage range, the highest frequency operation is obtained at higher supply voltages. Therefore, a 12 volt operating voltage was chosen, which is also a convenient battery voltage for portable operation. The series of eight BCD counters (4 dual counters) are connected in a ripple mode of operation.

The latches and BCD-to-7 segment decoders are configured with MC14511 devices. These CMOS parts have both latches with a strobe control and the decoder for a seven segment display with a blanking control pin for turning the displays off. This feature can be used to conserve the power drain by turning the displays off when there is no input signal. This is accomplished with 1/2 dual BCD counter C1 and flip-flop made from 2 input NAND gates G12 thru G15. If four reset pulses are received on the BCD counter with no input signal the displays are blanked out thus conserving power. If there is an input signal, C1 is constantly reset by Q1 of the first MC14518 counter, thus keeping the displays in the on state.

Multiplexing of the displays can be used at a slightly lower system cost and lower power dissipation, however, the package count is increased along with an increased circuit complexity. This topic is described in detail later in this note.

CONTROL

The function of the control section is to process the precise timing signals from the time base to provide the proper logic sequences to the counters and latches. The control section has four outputs. The first of these is the Enable line which turns the first counter on and off for the precise enable time period. The second is the Strobe line which transfers the count into the memory of the MC14511 latch decoder. The third control line is used for resetting the MC14518 decade counters to ready them for the next count cycle. The fourth is the display blanking line previously discussed.

If the counting cycle were run at the minimum enable time the count would be updated into the latches at this cycle time. In the case of a 10 μs time base the count would be updated at a 100 kHz rate. If the input frequency has any instability the last few digits of the display would change at the 100 kHz rate which would result in an unreadable flicker. Therefore the count cycle is operated at a much slower rate, in this case 0.1 second to 10 seconds depending on the setting of pot R2. Gates G3 and G4 make up a low frequency oscillator and gates G5 and G6 make up a one shot. The sequence starts with a 5 μs pulse from the one shot. This pulse toggles $\overline{Q}$ of FF1 low which removes the reset from the time base counters. This allows the time base counters to divide down the 1 MHz clock. Figure 4 shows a timing diagram of the resulting sequence. The enable input of the selected time base counter and three of its outputs, Q0 thru Q2, are shown. By "ANDing" Q1 and $\overline{Q}2$ together two pulses with starting edges equal to the desired time base are formed. The gate delays thru the time base are equal for both pulses, thus compensating for these delays. These pulses are applied to the input of FF3 which is 1/2 of a MC14013D dual flip-flop.

FF3 is wired as a toggle flip-flop of which the first pulse sets the Q output high and the second pulse resets it low. The three NAND gates G7, G8, G9 are used to decode the $Q1 \cdot \overline{Q}2$ from the desired time base counter. This counter is selected by the MC14512 or a 2 pole, 6 position switch may be used. The MC14512's are eight channel data selectors used to select one of eight channels of information via three bit binary control lines.

The flip-flop FF4 is used to insure that the edges of the enable pulse occur exactly with the 1 MHz clock pulses. Since the delays thru the time base and data selector are constant for both turn on and turn off pulses, these delays are cancelled and the waveform appearing at the $\overline{Q}$ output of FF4 is a precisely controlled time period. This time period is the enable or gating time.

The remaining functions to be performed during the counting sequence are the strobe pulse, counter reset pulse and control system reset pulse. These functions are derived with the MC14017 Johnson counter C2, flip-flop FF2, and associated gates. Until the end of the enable pulse, the Johnson counter is disabled thru either the clock line or the reset line. At the end of the enable pulse the Johnson counter is enabled and begins to count

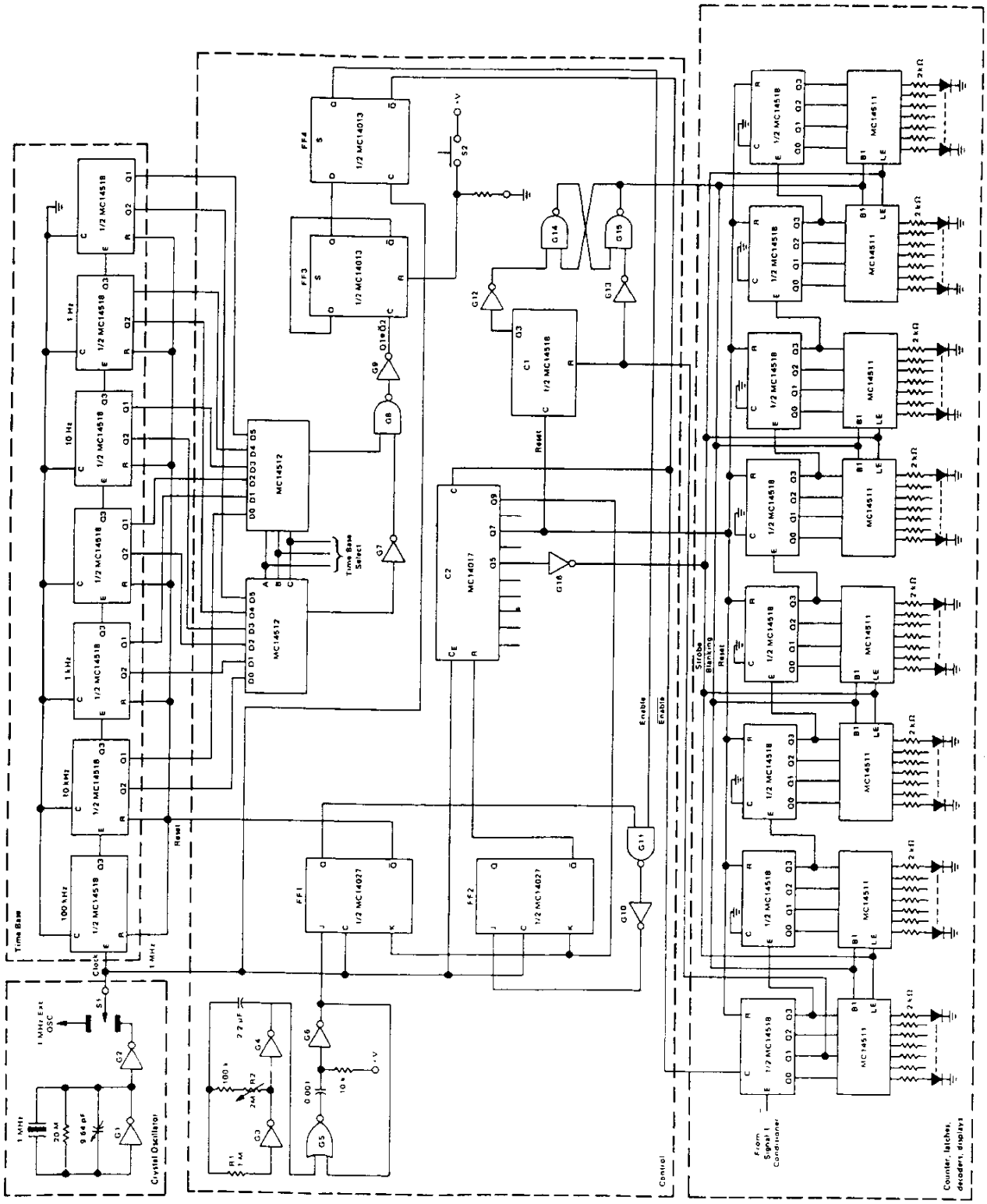

FIGURE 3 – BASIC 5 MHz COUNTER CONFIGURATION

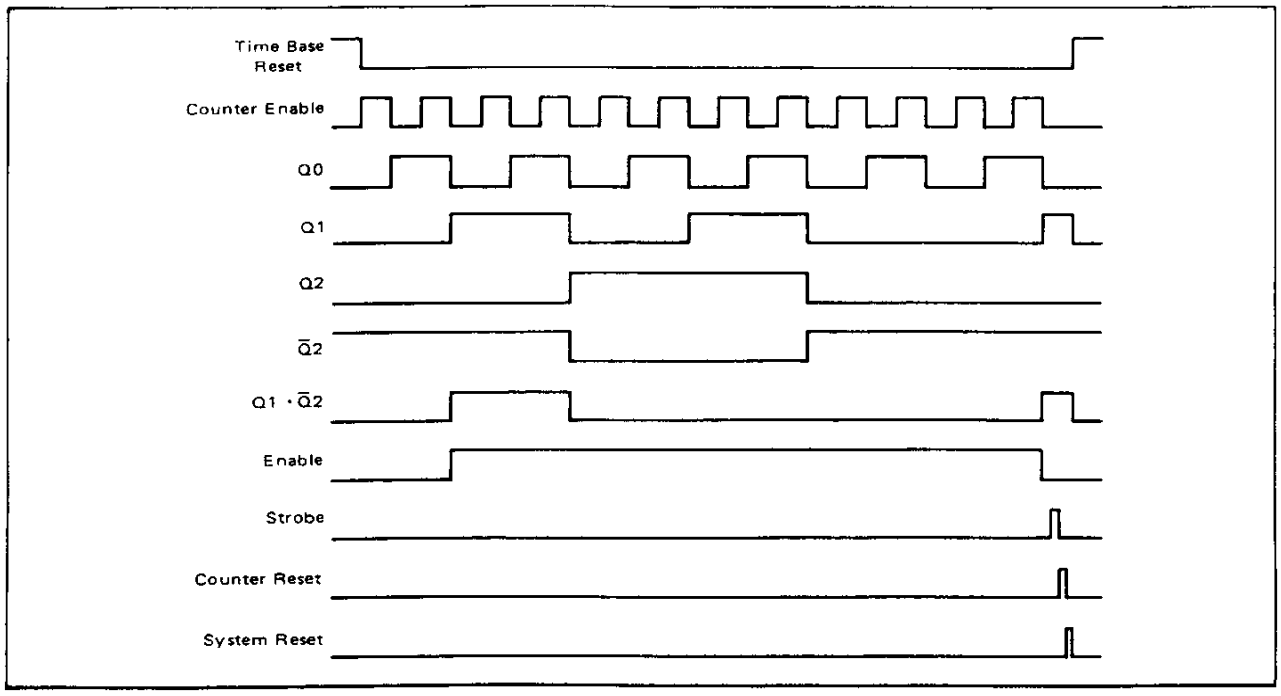

FIGURE 4 – TIMING DIAGRAM FOR BASIC COUNTER

the 1 MHz clock frequency. Of the 10 outputs of the counter, Q5 goes high for 1 μs after the 6th clock pulse. This pulse is used as the strobe pulse. After the eighth clock pulse Q7 goes high and the counters are reset. The tenth clock pulse resets the control system, via FF1 and FF2. Now the control system awaits another pulse from the low frequency oscillator and oneshot.

COUNTER FRONT END

The input signal for the basic frequency counter must swing from a logic "0" of zero volts to a logic "1" which in this case is about 10 volts. Therefore a functional block is needed to translate from any input waveform shape and waveform level to a signal that is capable of toggling the CMOS counters. Also the input to this block should have a high impedance so that the input waveform is left undisturbed by the frequency measurement. The contents of this block will contain a high impedance buffer with or without amplification connected with a Schmitt Trigger for waveform shaping. Also the input should be protected from very large signals.

The front end design chosen for this counter is shown in Figure 5. It consists of a FET and bipolar buffer followed by a Schmitt Trigger made from an MC75108 dual line receiver. This front end will operate up to 5 MHz with a 10 mV input signal.

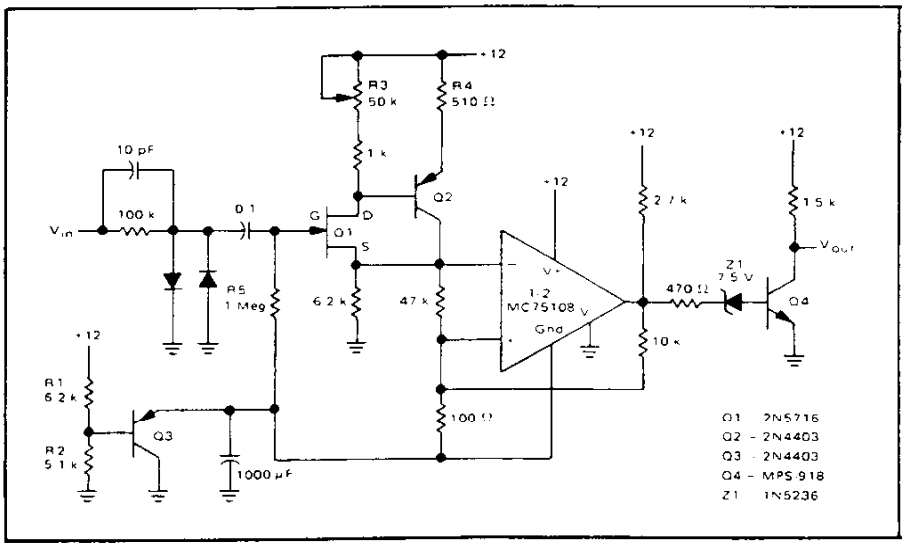

FIGURE 5 – 10 MHz FRONT END

The MC75108 line receiver is designed to operate from a ±6 volt power supply but can be biased up to operate from a single +12 volt supply. In addition to both a positive and negative power supply, the line receiver requires a ground connection at the midpoint of the supply voltages. The data sheet of the MC75108 indicates a typical positive supply current of 18 mA and a negative supply current of -8.4 mA. Thus the ground pin returns about 10 mA to the positive supply. For single supply operation the positive supply pin is connected to the +12 volt supply while the negative supply pin is connected to the counter ground. The ground pin on the line receiver must then be returned to a six volt reference capable of sinking up to a maximum of 15 mA. The PNP transistor Q3 and resistors R1 and R2 perform the function of a simple voltage regulator for the six volt reference.

The N-channel JFET Q1 and PNP bipolar Q2 provide a unity gain high impedance buffer for the line receiver. Potentiometer R3 adjusts the buffer output voltage to be equal to the six volt reference voltage for maximum sensitivity.

Under normal split supply operation, the output swing of the MC75108 is from 0 to the positive supply. Since the line receiver is biased up by six volts, the output swing is now from six to twelve volts. This voltage swing must be translated to voltage levels compatible with CMOS operating at +12 volts. This translation is done with the 7.5 volt zener Z1 and transistor Q4. When the output of the line receiver is at six volts the zener is off and Q4 is turned off. When the output of the line receiver is in the high state, Z1 is conducting and Q4 is turned on. The output voltage swings from cutoff to saturation of Q4 or about 0.5 to 12 volts.

The MC75108 is a dual line receiver. The power consumption of the package is constant whether both line receivers are used or not. Both line receivers in the package can be used to provide two separate input channels with a switch to select between them or they could be connected to the basic counter such that they were switched on and off alternating with each count cycle. Thus the first count cycle would look at channel "A" with the second count cycle looking at channel "B".

OPTIMUM POWER CONSIDERATIONS

Although the counter that has been described is capable of low power operation it was optimized for maximum performance. This optimization for maximum frequency and maximum sensitivity increase the power dissipation. For many applications the power dissipation is the most important consideration and decreasing the power consumption to the lowest amount may more than justify sacrificing the loss of frequency and sensitivity performance.

A power consumption optimization of the frequency counter should first include an analysis of where the major portions of the power is being consumed. Table 1 shows a performance comparison of the high performance counter previously discussed and the low power counter which follows.

Table 1 – Performance Ratings for Counters

	Maximum Performance	Minimum Power
Maximum Frequency	5.0 MHz	1.0 MHz
Sensitivity at above frequency	10 mV	120 mV
Basic counter power	10 mA	2.0 mA
Front end power (No input signal)	25 mA	6.0 μA
Front end power (1.0 MHz)	25 mA	180 μA
Display power	225 mA	70 mA
Power supply	+12 volt	+6.0 volt
Total current	260 mA	72 mA
Total power	3.12 watts	0.43 watts

The largest portion of this power is being consumed by the digital displays and thus the most obvious way to reduce the power consumption would be to choose the lowest power display type and optimize for it. However, it is not the intent of this article to discuss the subject of digital displays and their characteristics.

The displays chosen for this counter were Monsanto MAN-4 LED's because of their wide adaptability and their compatibility to the MC14511 seven-segment decoder driver.

In the basic counter previously discussed, the MAN-4's were operated at 4 mA per segment. While this current produces a bright and easily read display, a great deal of power is consumed in the displays.

Figure 6 shows a technique which multiplexes a single decoder driver between all of the displays and operates the displays at a lower power level.

Multiplexing of a digital display is a technique of time-sharing the circuit components and allowing the eye to integrate the readout over the total time period to make a display appear continuous. The multiplexing technique reduces the overall cost of the counter while increasing the complexity of the counter design. With the multiplex technique, the displays are then operated at a peak current of 20 mA but at a duty cycle of only 12.5%, which is a smaller power consumption. Also, the counter is operated at a six volt supply voltage which reduces the total power consumption.

Four MC14021 8-bit shift registers are used in the multiplexing technique. These shift registers have both parallel and serial inputs and permit not only a unique technique of multiplexing but also provide the latches that are required to store the count from the MC14518 counter chain.

The BCD outputs of the MC14518 counter chain are connected to the parallel inputs of the shift register. The least significant BCD bit of each of the eight counters is connected to each of the eight inputs of the first shift register. The next most significant bits of the eight counters are connected to the eight inputs of the next shift register. Therefore, with eight 4-bit BCD words, four 8-bit shift registers are required. The eighth output

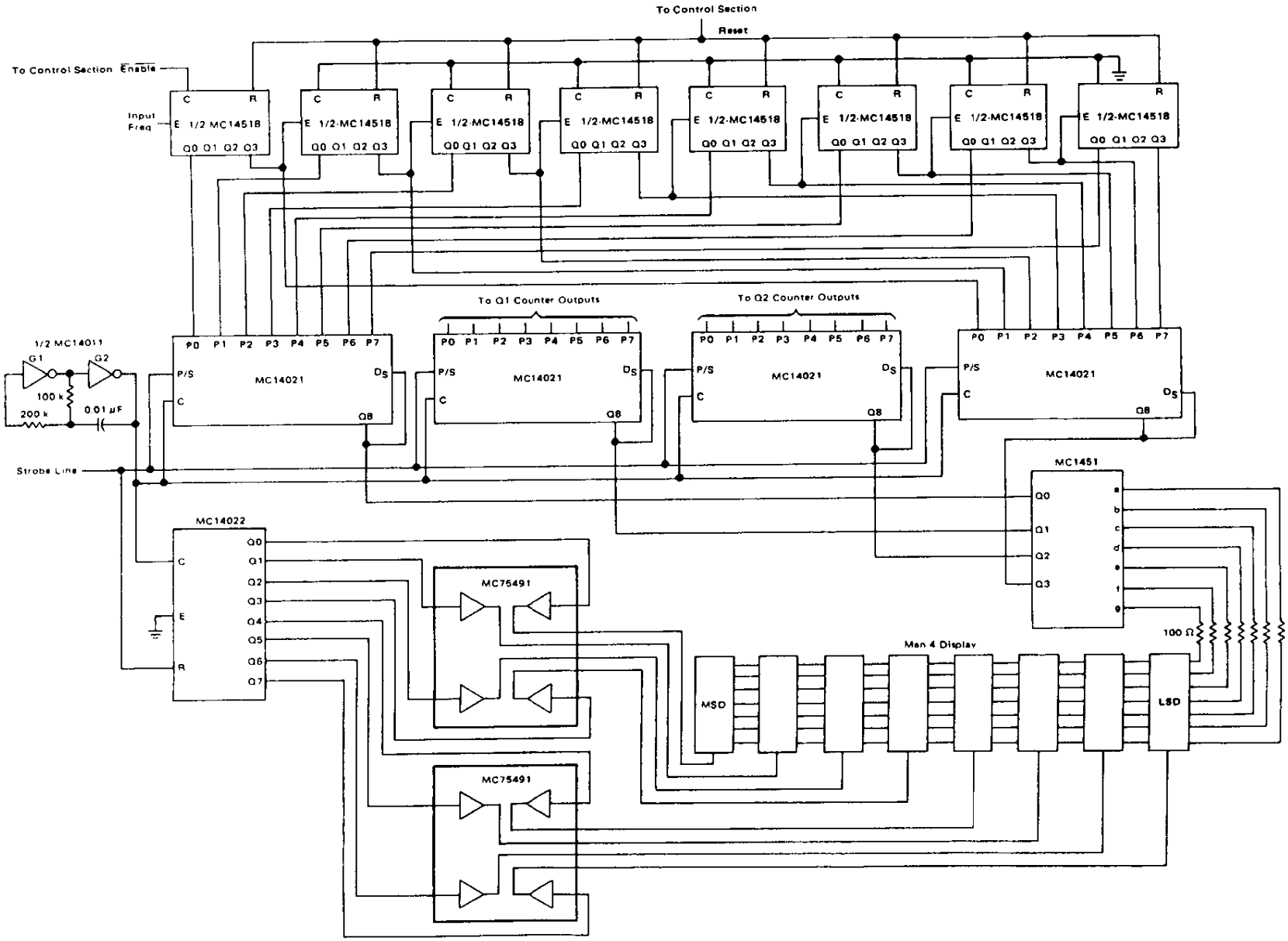

FIGURE 6 – A SINGLE DECODER DRIVER MULTIPLEXING APPROACH

of each shift register is connected to the series input of the same register so that the digital word in the shift register is shifted around in a loop from the first bit thru to the last bit.

When a logic "one" is applied to the parallel/series control line of the shift registers the digital information on the parallel inputs is loaded in the register. This control signal is the strobe pulse from the counter control section. Then after the register returns to series operation the digital word is shifted around thru the registers with each of the eight-bits of information appearing at the inputs to the single seven-segment decoder. An MC14022 octal counter/divider is used to keep track of which counter digit is presently being applied to the seven-segment decoder input. The clock signal for both digit selection and the shift register is derived from an oscillator constructed from gates G1 and G2. This oscillator controls the multiplex frequency and the values shown give a frequency of about 1 kHz. The outputs of the MC14022 digit selector are buffered through the MC75491 LED drivers to the MAN-4 display cathodes. The anodes of the MAN-4's are driven directly from the MC14511 BCD-to-7 segment decoder.

This technique represents an overall savings in both power and system costs with an increase in system complexity and a decrease in LED brightness.

Another area of possible reduction of power dissipation is that of the signal conditioning or front end. The front end previously described is optimized for maximum performance. This design not only requires about 25 mA of current from the 12 volt supply but this current is constant whether an input signal is present or not.

The circuit shown in Figure 7 is a low power front end for the counter. This design not only reduces the power consumption from that of the previous design but the power consumption is proportional to the input frequency. With no input signal to the front end, the current drain is only a few microamps. This counter front end design uses 1/2 of an MC14583 CMOS Schmitt Trigger which operates from the single six volt power supply used in the lower power counter. A single resistor, R1, is used to set the threshold voltages from both the high and low logic states. The over voltage protection network that is used with the high performance front end is also used in front of the MC14583 Schmitt Trigger.

The reduced power consumption is not gained without sacrificing overall performance. Both input sensitivity and the upper frequency limit is decreased. When using the CMOS MC14583 Schmitt Trigger for the counter front end the upper frequency limit is about 3 MHz with an input sensitivity of 400 mV. However, the overall power consumption of the front end is considerably reduced. Figures 8 and 9 show the sensitivity versus input frequency curves for both the low power and high performance version of the counter.

Both of these frequency counters were designed for battery or portable operation. Again, referring to Table 1, the power requirements are listed for each of the counters. From this information the desired battery can be chosen for maximum operating period and minimum size.

There are many types and sizes of batteries available for operation of these counters. The battery may be a throw away non-rechargeable unit or one of the many types of rechargeable units. In the case of the rechargeable battery, the method of battery charging depends upon the type of battery and may be as simple as a transformer, rectifier and current limiting resistor or a very complex unit with discharge indicators, timing circuitry or automatic recharge circuitry. The manufacturers of the desired battery should be consulted as to the method of charging compatible to that type of battery. Also, Motorola application note AN-447 deals with Ni-Cad battery charging.

For the lab prototype counters, a GC1245 12-volt battery and a GC626 6-volt battery manufactured by Globe Battery were chosen for the 12 and 6-volt counters. The 12-volt battery has a capacity rating of 4.5 Ah. This will allow about 17 hours of continuous operation with the higher performance counter. The six-volt battery has a capability of 2.6 Ah which will allow approximately 32 hours of continuous operation from the lower power counter. This six-volt battery weighs about a third that of the 12-volt battery thus offering a smaller total package.

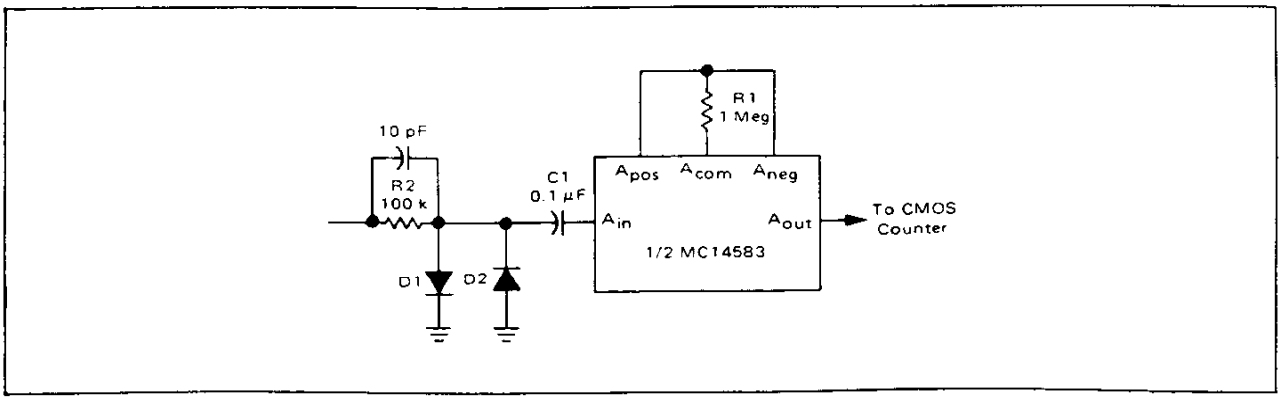

FIGURE 7 – LOW FREQUENCY FRONT END

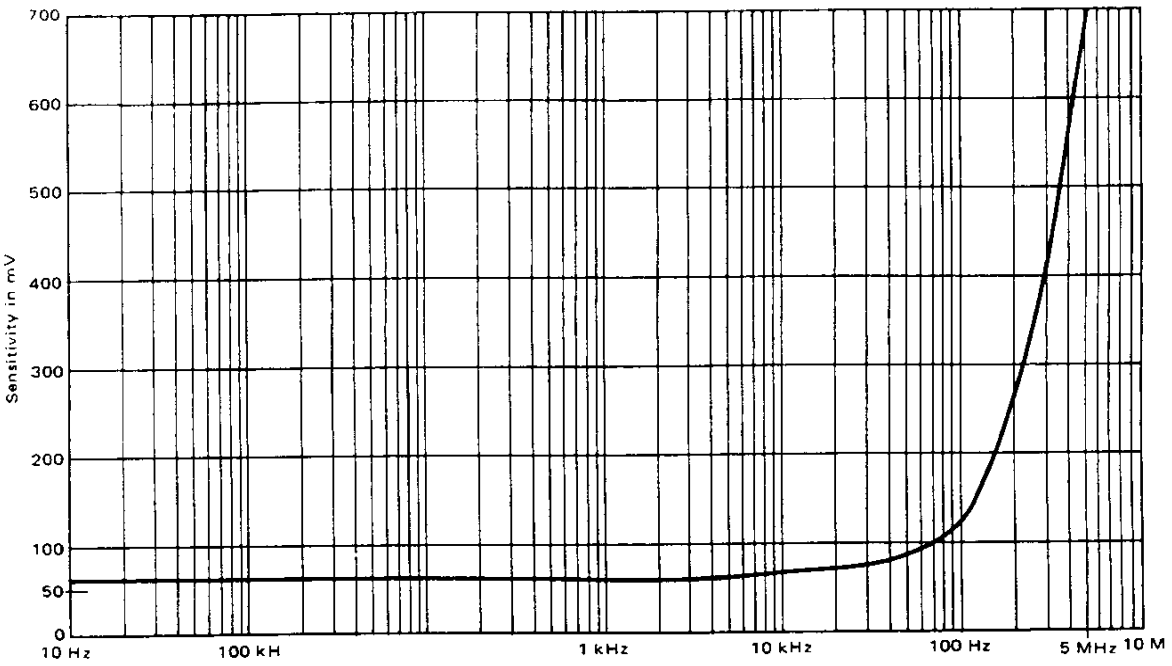

FIGURE 8 – SENSITIVITY Versus FREQUENCY CMOS FRONT END AND CMOS COUNTER V_{DD} = 6 V

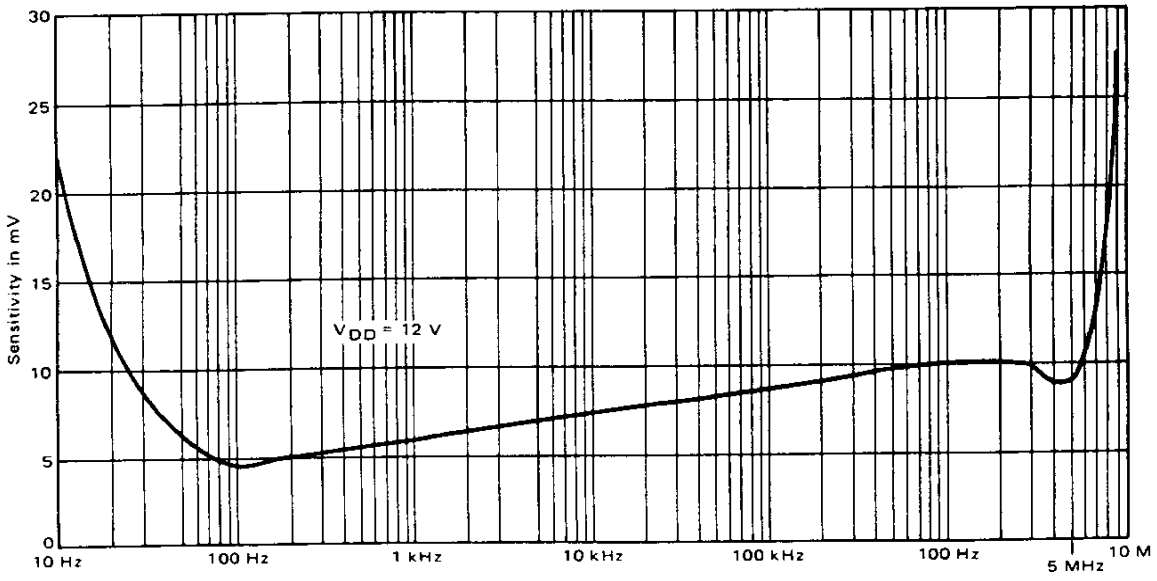

FIGURE 9 – SENSITIVITY Versus FREQUENCY FOR LINEAR FRONT END AND CMOS COUNTER

CONCLUSIONS

The advantages of a low powered logic family such as CMOS can be used to provide a battery operated frequency counter for use in both portable equipment and applications where the power source capability is limited. This application note has presented two versions of a frequency counter, both of which are designed for battery operation. The first circuit design optimizes the counter for maximum frequency and sensitivity performance from the CMOS logic family while the second counter minimizes the power dissipation to produce the maximum operating time from a battery power supply. The circuit details are presented as well as the performance data on the lab prototype frequency counters.

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MOTOROLA

JIT PRINTED IN THE USA 1993 MPS

AN717/D