AN-708A
Application Note

LINE DRIVER AND RECEIVER CONSIDERATIONS

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This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

MOTOROLA *Semiconductor Products Inc.*

LINE DRIVER AND RECEIVER CONSIDERATIONS

INTRODUCTION

The relatively new field of data communications has generated the need for many new integrated circuit functions. A good example of this point is found in the important area of system interfacing, where it is necessary to transmit high speed data streams from one system to another. The distances involved may vary from a few feet to several thousand feet.

In recent years, a new family of integrated circuits has evolved to fulfill this need. These devices are called line drivers and receivers. These specific components form the basis for this note. Emphasis is placed on subject material, such as transmission system description, IC description, important IC parameter description, noise consideration, line considerations, and applications.

SYSTEM DESCRIPTION

A brief description of transmission line systems that use line drivers and receivers is presented to provide an overall "picture" of the system and data paths involved.

A basic driver/receiver transmission system is shown in Figure 1. Here an input data stream (V_{in}) feeds a driver, which in turn drives a line. Information at the other end of the cable is detected by the receiver that provides an output data stream, usually of the same logic level as V_{in}.

The line involved could be a single line, a coaxial cable, a twisted pair line, or a multi-line cable. The latter could be of the ribbon cable type, multi-twisted pair type, etc. The line could be operated in a single-ended or differential mode.

Another common driver/receiver system, shown in Figure 2, is commonly called a "party-line" or "bus" system. Here, the line is shared by drivers and receivers. It should be pointed out that although any driver can be utilized to drive the line, only one driver can be used at any one time.

LINE DRIVER

The line driver commonly translates the input logic levels (TTL, MOS, CMOS, etc.) to a signal more suitable for driving the line. An important exception to this is found in the MECL logic family, where MECL gates may be used to drive the line directly.

A popular method of driving lines between TTL systems is the differential-open collector approach (see Figure 3). Using this technique, first transistor Q_1 pulls current (sinks current) through R_1 from ground. This, for instance, could correspond to the input logic level going "high". When the input logic level goes "low," Q_2 will conduct and pull current through R_2. Thus, a voltage

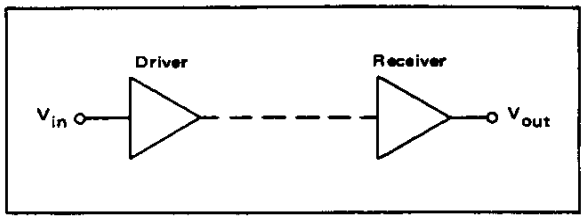

FIGURE 1 – Typical Line Driver-Receiver System

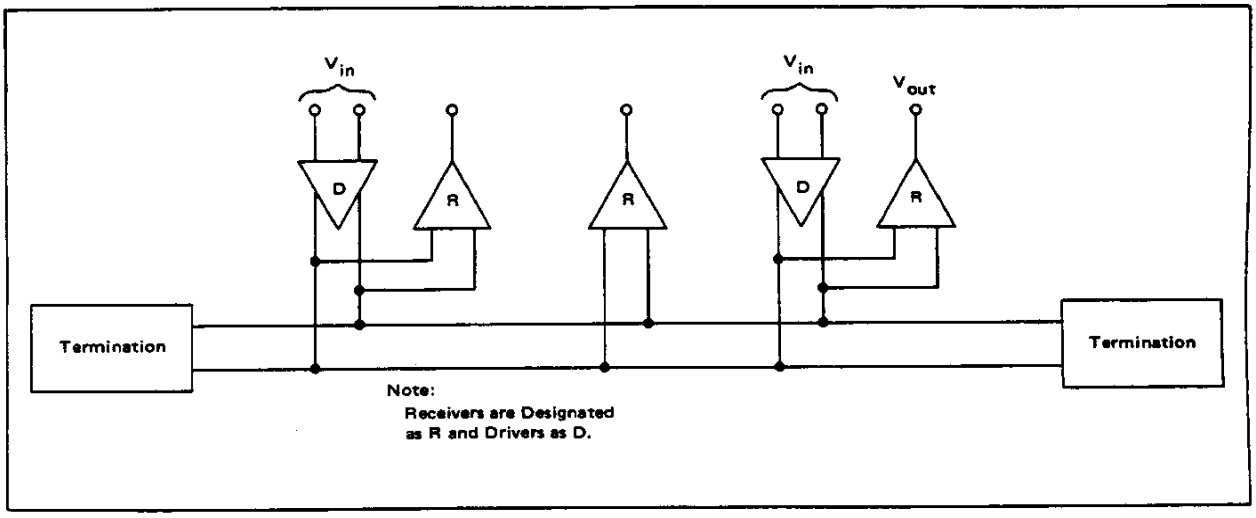

Figure 2 – Typical "Party-Line" or "Bus" System

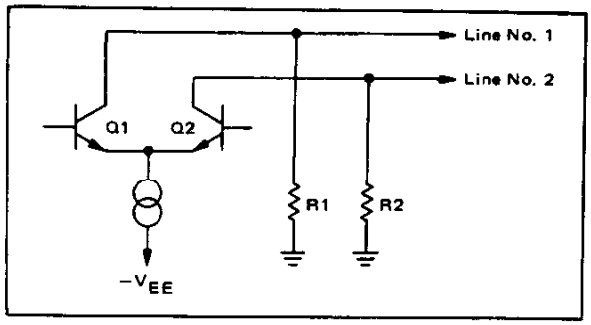

FIGURE 3 – Basic Pull-Only Circuitry Utilized by MC75110

differential, which is a function of the line terminations, is created on the line.

It is important to note that one line is always at ground potential. Thus, line #1 goes low when Q_1 conducts, but line #2 remains at ground potential, since Q_2 is off. Likewise, when Q_2 conducts, line #2 goes low and line #1 is at ground potential. An example of an IC driver utilizing the pull-only technique is the MC75110.

The MC75110 has the additional feature of a strobe or gating input. This feature allows the line driver current sources to be turned-off regardless of the input signal. Strobe capability has important advantages in party-line applications.

Other types of drivers include balanced differential voltage drivers (see Figure 4) such as the MC3487, which

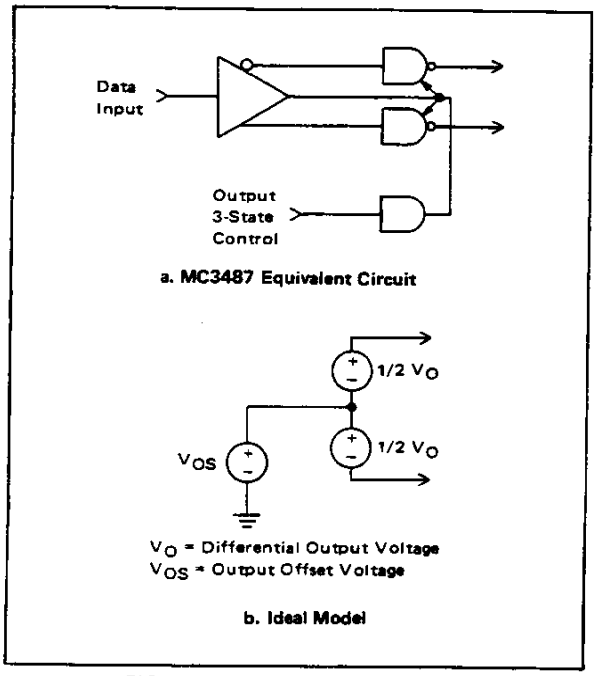

FIGURE 4 – Differential Voltage Driver

is compatible with EIA Standard RS422. In this type of circuit, the outputs are switched so that for a logic 1 input, output A > output B; for logic 0 input, output B > output A.

To allow devices of this type to run on a single power supply, the outputs are switched between ground and some upper voltage which is less than the power supply voltage. This type of operation can be modeled as shown in Figure 4b. The output offset voltage (V_{OS}) of the driver is the algebraic mean of the output voltages measured with respect to ground. The differential output voltage (V_O) is the difference between the two output levels.

The third type of driver is the single-ended voltage driver. The output of this type of driver is either positive or negative, with respect to the driver's ground, depending on the input. Figure 5 shows this type of driver and the

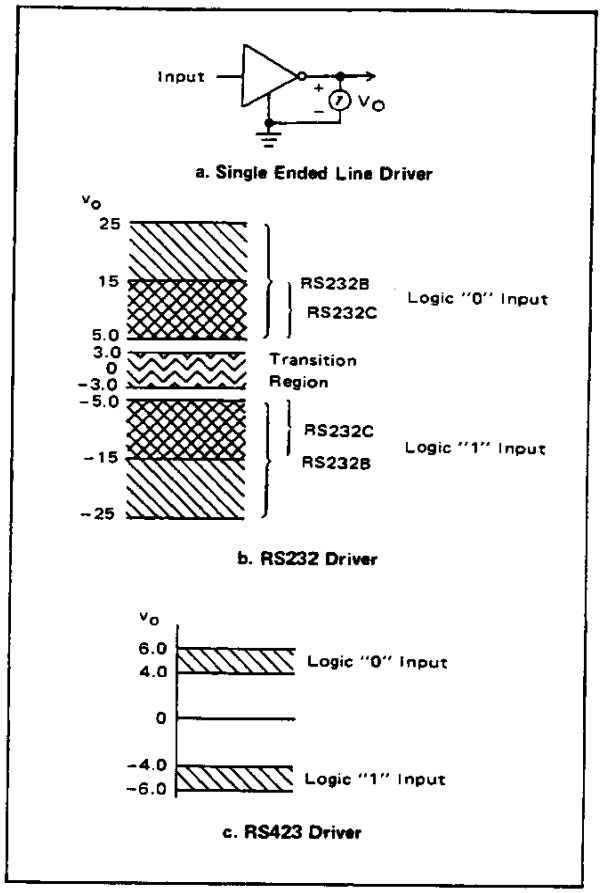

FIGURE 5

associated output levels for EIA Standards RS423 and RS232.

It should be noted that a negative output voltage represents a mark or binary 1. Therefore, if an inverting driver such as the MC3488 or MC1488 is used, a positive logic input such as TTL will produce the appropriate output voltage without additional inverters. The MC1488 and MC3488 are compatible with EIA Standards RS232 and RS423, respectively.

LINE RECEIVER

The line receiver provides the reverse function of a line driver where the voltage previously applied to a line is now detected and restored to an output logic level. This function may be performed by various digital and linear

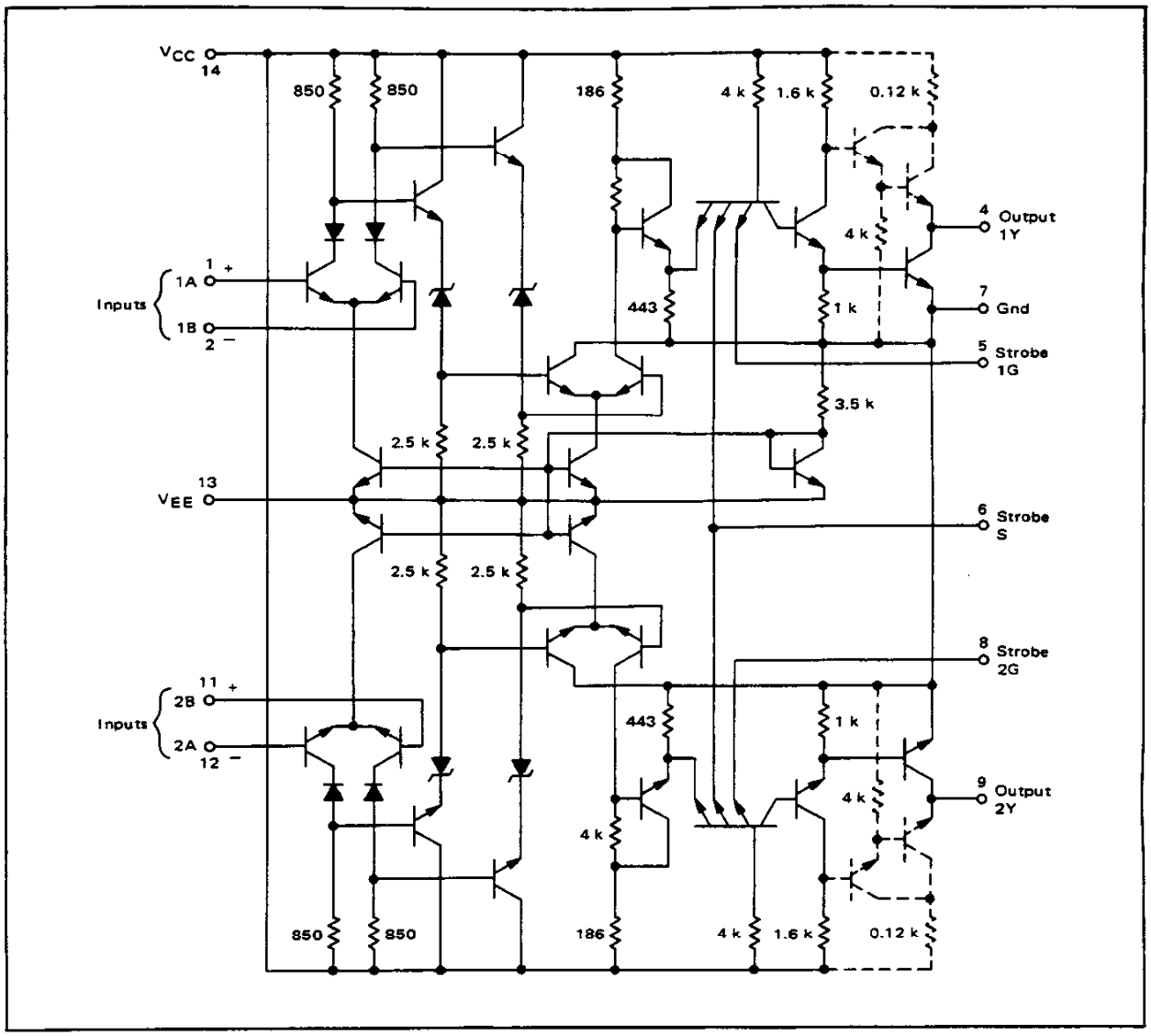

FIGURE 6 – MC75107 Line Receiver

IC's. Simple examples of this include comparators and gates. The latter includes a group of IC's specifically designed as line receivers that combine linear and digital techniques. These IC's use linear circuitry to detect the output signal from the cable. This signal level may be quite small (less than 100 mV) with considerable noise. The digital circuits provide the necessary drive to interface with any of the common digital logic families, such as TTL, CMOS, MECL, etc.

An example of a line receiver is the MC75107 (see Figure 6). This receiver utilizes a differential input stage to provide a high-input impedance and common-mode noise rejection. This stage is followed by a level shifting stage and a second differential amplifier. The output stage provides TTL logic levels.

Since each receiver shunts the line, it is important to know the amount of loading contributed by the receiver. That is, how much resistance and capacitance is shunted across the line due to the input impedance of the receiver. Any significant loading of the line will result in undesirable reflections.

Typical input impedance of the MC75107 is shown in Figure 7. Data for two frequencies, 5 MHz and 10 MHz, versus input level is also shown.

From this data, it can be seen that the input impedance increases with signal level. Even at minimum signal levels (30 mV) and maximum operating frequency (10 MHz), the equivalent parallel resistance is typically 1000 ohms. This is an order of magnitude higher than the typical characteristic impedance of many lines.

Similar data for other parts are shown in their respective data sheets.

The term "common-mode voltage" or noise is used in relation to receivers with differential input stages. Ideally, a difference amplifier will amplify only the difference of two voltages appearing at the input terminals. If both

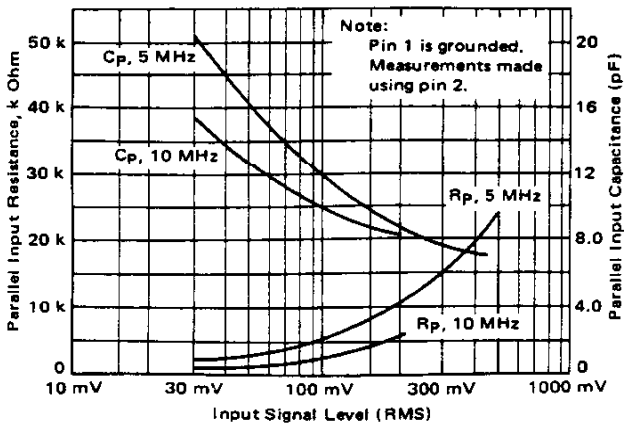

FIGURE 7 – Parallel Input Impedance of MC75107 versus Signal Level (RMS)

input terminals are driven with the same polarity signal with respect to ground, the amplifier will attenuate rather than amplify the signals. Identical signals of this type are called common-mode input voltages, or common-mode noise.

Mathematically, the common-mode voltage is defined as the algebraic mean of the two input signals measured with respect to ground. Common-mode noise often appears as external noise of the same polarity, induced equally in both conductors of a differential transmission system. Thus, if the receiver utilizes a differential input stage, this common-mode noise is attenuated.

The common-mode voltage range is the range over which a differential amplifier will properly attenuate the common-mode signals. For example, the recommended operating conditions of the MC74107 specify a common-mode voltage range of −3 to +3 volts. Common-mode voltages within this range will be attenuated.

DUPLEX SYSTEMS

Duplex transceivers such as MC10194 are capable of simultaneous bidirectional data transfer. To accomplish this, current mode drivers are used in a manner such that one of three voltage levels may appear on the line corresponding to one of three conditions:

a. Both drivers off.
b. One driver on.
c. Both drivers on.

Each driver inhibits data being transmitted by it from appearing on its receiver's output. For a more detailed discussion of duplex transceivers see the MC10194 data sheet.

NOISE CONSIDERATIONS

Noise is an important consideration in the line transmission of digital data. Where noise appears and how it influences the system will depend largely on the overall transmission line system used. This section discusses noise in several single-ended and differential transmission line systems.

Noise generally appears in two primary places in line driver/receiver systems: one, in the ground system, or two, directly on the line. How much this noise degrades the signal-to-noise ratio appearing at the input terminals of the line receiver depends on the transmission system selected.[1]

A simple single-ended system using one driver and one receiver is shown in Figure 8. Here, a single wire is utilized to transmit the data signal. This system is particularly prone to both ground and induced* noise; that is, any induced noise on the line will add to or subtract from the signal. Likewise, any ground noise between ground 1 and 2 will add or subtract from the signal. Regardless of the source of the noise, the overall signal-to-noise ratio appearing at the input of the receiver is degraded.

One solution to this degradation of signal-to-noise ratio is to increase the signal level. A direct implementation of this technique is to use high-threshold logic such as MHTL. This approach requires higher supply voltages as well as increased power.

Another possible solution is to use a shielded center conductor, coaxial cable. This approach successfully shields the line from induced noise but, the problem of ground noise remains with increased chance for data transmission error.

A third approach is to use a single ended driver and a differential receiver in an unbalanced system as shown in Figure 9. Since one of the receiver's inputs is connected to the driver's ground, any ground noise between the receiver and driver will add to the common-mode voltage of the receiver. In addition, noise induced in the line will likely appear on both lines and also add to the common-mode voltage.

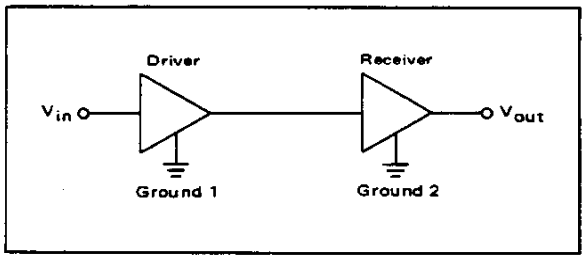

FIGURE 8 – Basic Single-Ended System

The second basic transmission system is the differential configuration (see Figure 10). Since terminating the line is necessary to minimize reflections, terminating resistors are shown. Lines are balanced in a differential system; therefore, externally-induced noise will appear equally on both inputs to the line receiver. The receiver uses a differential input stage to respond primarily to a differential signal, rejecting common-mode noise. This rejection of common-mode noise (as well as a reduction of ground noise) offers a significant advantage over the single-ended approach.

Although the rejection of common-mode noise is of

*Induced noise here refers to that noise induced from nearby equipment, such as relays, etc.

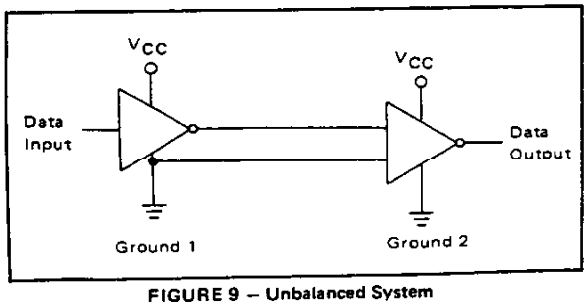

FIGURE 9 – Unbalanced System

paramount importance, the differential system also offers some immunity to differential-mode noise. The degree of differential noise immunity depends on several factors, such as, line impedance, the matching of termination resistors, driver current capability, line length, and the clock frequency.

The following example demonstrates how differential-mode noise margin may be calculated for a given system. For simplicity, an ideal system is considered where only the characteristic impedance of the line, Z_o, and the driver current capability, $I_{o(on)}$, are included. With this system, the transmission line is terminated in Z_o at both ends of the line. The assumption is also made that the driver is a pull-only type. Thus, the total drive current, $I_{o(on)}$, for a particular logic state is effectively split between one terminating resistor at the driving end and another at the receiving end.

Therefore the voltage driving line A, V_1 (see Figure 11) is:

$$V_1 = \frac{I_{o(on)}}{2} \times \frac{Z_o}{2} \qquad (1)$$

or

$$V_1 = \frac{I_o Z_o}{4}$$

Since the line is assumed to be short enough to neglect line loss, V_1 is also the input to the receiver ($V_1 = V_2$). When line B goes low during the other half of the input logic swing, V_1 assumes essentially the same value with an opposite polarity.

If the following assumptions are made, we can plot noise margin (see Figure 12) for a typical line receiver such as the MC75107.

Z_o = 170 ohms

$I_{o(on)}$ = 6.9 mA (minimum value at 25° C)

Receiver threshold = 50 mV

$$V_1 = \frac{I_o Z_o}{4}$$

$$V_1 = \frac{(6.9)\ (170)}{4}$$

$$V_1 = 293 \text{ mV}$$

The noise margin from Figure 12 is:

Noise margin = 293 mV - 50 mV

= 243 mV

These values of noise margin assume that the clock frequency and/or line length is small enough to neglect signal attenuation by the line.

For a differential receiver to properly attenuate common-mode signals, the receiver must operate within the allowable common-mode range. The following example illustrates how noise can affect the common-mode voltage.

For simplicity, an ideal voltage driven differential system will be considered. Figure 13 shows a differential system and sources of noise. V_G in the diagram represents the difference in ground potential between the driver and receiver. V_I represents the induced common-mode noise on the line.

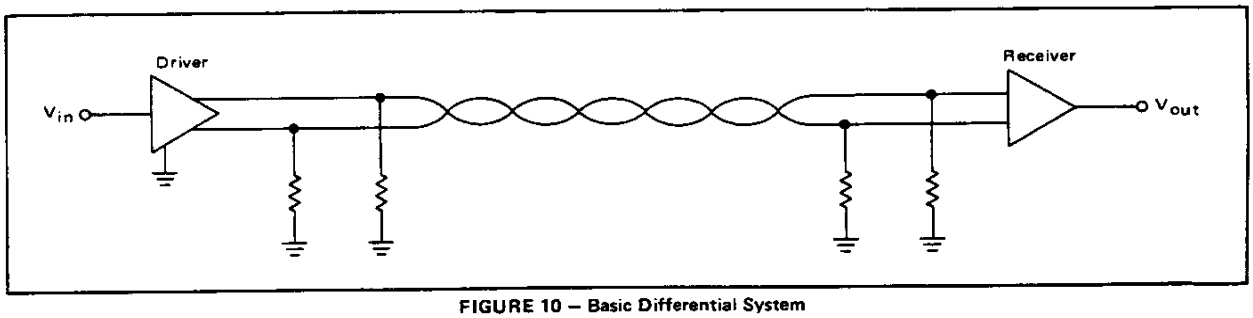

FIGURE 10 – Basic Differential System

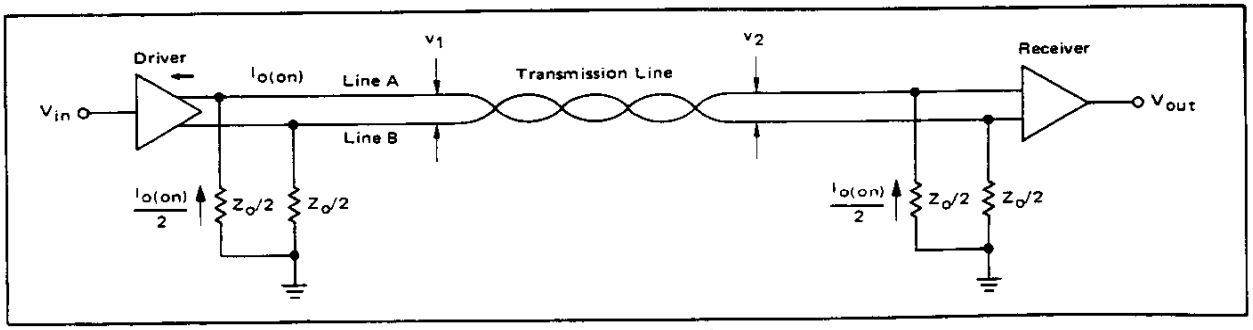

FIGURE 11 – Differential System Showing Currents

The common-mode voltage at the receiver is:

$$V_{CM} = V_{OS} + V_G + V_I$$

If the allowable characteristics are:*

$$|V_{OS}| < 3\ V$$

$$2\ V < |V_O| < 6\ V$$

$$|V_G + V_I| < 4\ V$$

then the required common-mode range is:

$$V_{CMR} = \pm V_{OSmax} \pm (V_G + V_I)_{max} = \pm 7\ V$$

Thus the receiver must have a common-mode range of at least ±7 under these conditions.

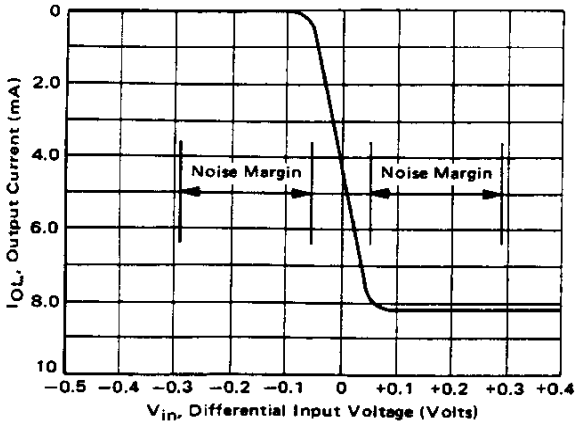

FIGURE 12 – Noise Margin of MC75107

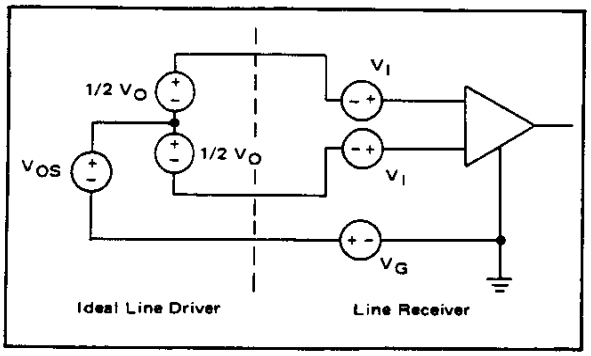

FIGURE 13 – Differential System Showing Noise Sources

LINE CONSIDERATIONS

Since the medium of transmission is a line, it is important to understand how the transmission line distorts the data stream or more specifically the individual pulses. Although it is not the intent of this note to discuss all the idiosyncrasies of a transmission line, it is important to point out several significant line characteristics. More detailed information can be obtained from the bibliography.

A good starting point is to examine the attenuation characteristics of coaxial cable, and then to extend these characteristics to twisted pair, ribbon cable, etc. The two major sources of loss in a coaxial cable are conduction loss in the dielectric and resistive loss in the center conductor.[2,3,4] Below 1 GHz, the attentuation is predominately determined by the resistive loss of the center conductor. This resistive loss is a function of the diameter of the center conductor. In addition, because of skin effect, it also varies as the square root of frequency. Thus, larger cables with consequently larger center conductors have less resistive loss. With a given line, however, the resistive loss varies as the square root of frequency. An example of this resistive loss or attentuation versus frequency for several lines is shown in Figure 14. Included with the coaxial cables is a twisted pair line. The twisted pair line shown, although having more attenuation, exhibits the same square-law characteristic as the coaxial cables. That is, the slope of the curves in Figure 14 is essentially the same. These curves approximate the square root function of attenuation versus frequency ratio previously discussed. viously discussed.

If curves of the type shown in Figure 14 are not readily available, it is relatively simple to measure the attenuation of the unknown line at the desired clock frequency. A simple way to do this is to drive the line single-ended with a pulse generator operating at the desired clock frequency. A scope can then be used to measure the input signal into the cable and the signal coming out the other end of the cable when terminated in its characteristic impedance. The recommended method of measuring the characteristic impedance is to use the time-domain reflectometer[1] (TDR) technique. The determination of the attenuation and characteristic impedances are essential in designing a driver-receiver system.

Since the data stream consists of an irregular series of pulses, another important consideration is the step response of the cable. That is, what effect does a cable have on an input pulse with a fast rise time, and how much does the cable attenuate this single pulse. The assumption here is that we are discussing one pulse. This could correspond to the situation where the driver input receives a "1" and a long series of "0's".

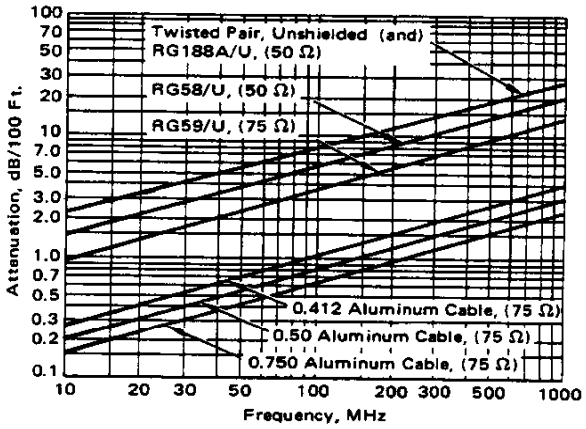

FIGURE 14 – Attenuation versus Frequency

*Driver characteristics are compatible with EIA RS422.

Dreher[5] shows that:

$$E_{out}(t) = E_o\left[1 - \text{erf}\frac{\ell K}{4R_o t^{1/2}}\right] \qquad (2)$$

where E_o is the magnitude of the input step and $E_{out}(t)$ is the magnitude of the output pulse as a function of time.* The term K is a constant associated with the line. Likewise, R_o and ℓ refer to the line and are the characteristic resistance and length, respectively.

Equation 2 can be solved for the time "T_o", necessary for the magnitude of E_{out} to reach 50% of the input pulse magnitude. The value of "T_o" for a line may be calculated from:

$$T_o = 4.56 \times 10^{-7}\frac{(a_o\ell)^2}{f_o} \qquad (3)$$

where

a_o = attenuation, dB/100 ft.
f_o = frequency, Hz
ℓ = cable length, ft.

A modified version of equation 3 is:

$$T_o = \frac{(4.56)(a)^2}{f}10^{-9} \qquad (3a)$$

where

a = total attenuation of line, dB
f = frequency, MHz

Equation 3a is convenient when the attenuation is measured directly—rather than read from a curve or table. A further simplification of equation 3 is:

$$T_o = \frac{1}{(6.1)(f_6)} \qquad (3b)$$

where

f_6 = frequency (Hz) where the total attenuation is 1/2 or 6 dB.

The frequency (f_6) is determined by adjusting the input signal clock rate so that the magnitude of signal appearing at the output of the line is reduced in magnitude by 2 (i.e., 6 dB).

For example, the value of f_6 for 612 feet of unshielded twisted pair line (see Figure 21 for description) is determined to be approximately 1.5 MHz. Thus T_o is:

$$T_o = \frac{1}{(6.1)(1.5 \times 10^6)} = 109 \text{ ns}$$

The actual measured value of "T_o" for this line is found to be 115 ns.

The expression shown in Equation 2 is too complicated to use. Kerns[2] has, however, provided solutions of Equation 2 for various ratios of E_{out} and E_o. This data is shown in Figure 15. Remembering that "T_o" is the time for the output pulse to reach 50% of the input pulse magnitude, then in Figure 15 it takes 29 times this value of "T_o" to reach the 90% value.

*Time (t) is assumed to start after the line propagation delay from the injection of the step into the line.

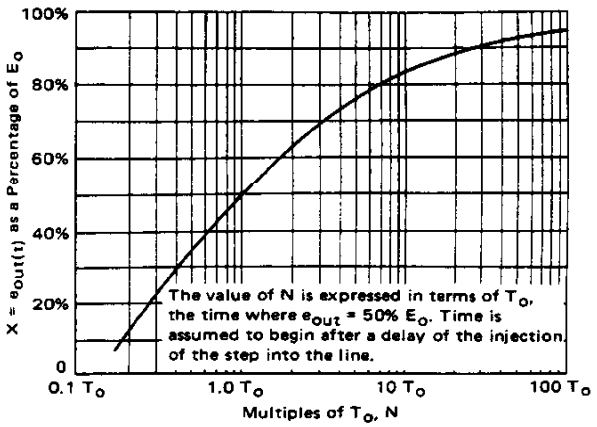

FIGURE 15 — Curve Showing $e_{out(t)}$ (as a percentage of E_o) versus N

Two examples are shown to point out the use and value of Figure 15. First, Figure 15 can be used to determine the rise time of a pulse, after passing through a cable of known characteristics. The time necessary for the output pulse to reach 10% of the input pulse can be found from Figure 15[2,5] by entering the curve at a value of "x" equal to 10% and reading a value of "N" equal to 0.17 "T_o". Likewise, the 90% value is 29 "T_o". Thus, the time for the output pulse to go from 10% of the input pulse magnitude to 90% is:

$$29 \text{ "}T_o\text{"} - 0.17 \text{ "}T_o\text{"} = 28.83 \text{ "}T_o\text{"}$$

If the line constants are known, "T_o" can be calculated and thus the rise time of the output pulse can also be calculated.

The second example, using Figure 15, calculates how much a pulse of known width is attenuated. For example, assume the same cable used previously to calculate a typical value of "T_o", is used again. The value of T_o calculated was 109 ns. If the pulse width is 136 ns, then the value of N is:

$$\frac{136 \text{ ns}}{109 \text{ ns}} = 1.25 \text{ or } 1.25 \text{ "}T_o\text{"}$$

The value of X from Figure 15 for 1.25 "T_o" is approximately 55%. That is, for a pulse width of 136 ns, the output pulse magnitude is only 55% of the input pulse, or the input pulse is attenuated approximately 5.2 dB by the cable.

Thus, Figure 15 provides the information necessary to calculate the rise time of a pulse after passing through a cable of known length and characteristics. In addition, the attenuation of a single pulse by a cable of known length and characteristics can also be calculated.

In the previous discussion, the effect of the cable for low duty cycles was determined. Specifically, the situation was discussed where the input data stream was essentially a "1" followed by a long series of zeros (i.e., one pulse). In this section, the situation where the input data stream is a long series of alternate "ones" and "zeros"; that is, a continuous pulse train, as shown in Figure 16 will be discussed. For purposes of simplicity and discussion, the

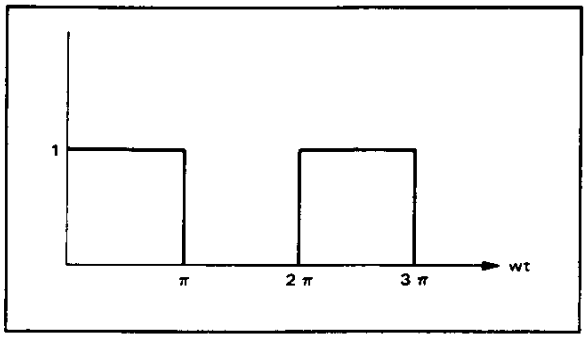

FIGURE 16 – Pulse Train, 50% Duty Cycle

assumption is made that this pulse train has a 50% duty cycle.

The Fourier-series representation of this pulse stream[6] is as follows:

$$f(\omega t) = \frac{2}{\pi}\left[\frac{\pi}{4} + \sin \omega t + \frac{1}{3}\sin 3\ \omega t + \frac{1}{5}\sin 5\ \omega t + \ldots\right] \quad (4)$$

This series consists of a dc component plus several frequency components. The first frequency term, sin ωt, corresponds to the basic clock frequency. The other terms correspond to the third, fifth, etc. harmonics of sin ωt. If the duty cycle is reduced slightly, the even harmonics appear also. In addition, the magnitude of each frequency, even or odd, will change. Since the dc component is the average, it also changes with duty cycle.

An example of how the frequencies add together with the dc component to form the pulse stream is shown in Figure 17.[6] The Fourier-series provides a convenient method of analyzing the effect that a cable has on a continuous pulse train. The line used to transmit a pulse stream, of course, will cause distortion. This distortion depends on how each of the terms or frequencies are attenuated by the cable. If each frequency is attenuated the same amount by the cable, the resultant wave shape would be identical to our input data stream – only attenuated a fixed amount. Unfortunately, the cable does not attenuate each frequency by the same amount – as demonstrated in Figure 14. Consequently, the relative magnitudes of each term in equation 4 are changed. If the attenuation of the magnitudes of each of the frequencies (sin ωt, sin 3 ωt, etc.) of equation 4 is known, the resultant wave shape can be reconstructed in a manner similar to that shown in Figure 17.

Equation 4 also demonstrates another important consideration. That is, that the relative magnitude of the pulse stream is primarily determined by the fundamental frequency (i.e., sin ωt). This approximation can be used to determine how much a particular line length attenuates the magnitude of a known input pulse stream. For example, if 600 feet of twisted pair line attenuates a 10 MHz sinusoidal signal 15 dB, then a pulse train with a clock rate of 10 MHz will also be attenuated 15 dB.

As the maximum clock frequency increases, the cable will eventually attenuate the higher frequencies to the point where the output is primarily a sine wave with a dc offset. This dc offset voltage is equal to the average

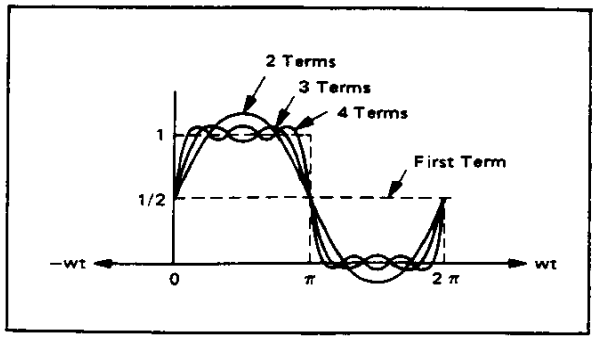

FIGURE 17 – Adding Components of Fourier Series

value of the input-pulse stream, ignoring dc resistance of the line. As previously mentioned, this dc offset voltage varies directly with the duty cycle. Thus, as the frequency increases, the output decreases symmetrically in magnitude about a dc level. This offset phenomenon can be particularly troublesome in driver/receiver systems where its value may exceed the threshold of the receiver. That is, the receiver may be biased "on" or "off" by the dc offset voltage. A detailed example of how this dc offset voltage affects a typical differential system is discussed in the Applications system.

Another important parameter of the line is the characteristic impedance. Actually, depending on the type of line, two distinct characteristics may be exhibited.[7,8] The common-mode characteristic impedance, often called "even-mode" (Z_{oe} or Z_{cm}), is due to the two lines being at the same potential and carrying equal currents in the same direction. The differential mode characteristic impedance, Z_{dm}, commonly called "odd-mode", is due to the lines being at equal but opposite potentials, and carrying equal currents in opposite directions. The expression often used for this mode is Z_{oo}. For the purpose of this report, Z_{dm} is equal to twice Z_{oo}.

For the simplified situation using a coaxial cable (one center conductor) or an unshielded twisted pair, only one mode applies. However, for shielded twisted pair, ribbon cable, and multi-conductor cable where lines are used as grounds, both modes must be considered. That is, the lines must be terminated so that both modes of signals will be absorbed rather than reflected at the termination points.

The differential mode characteristic impedance of a particular line may be measured[10] from the circuit in

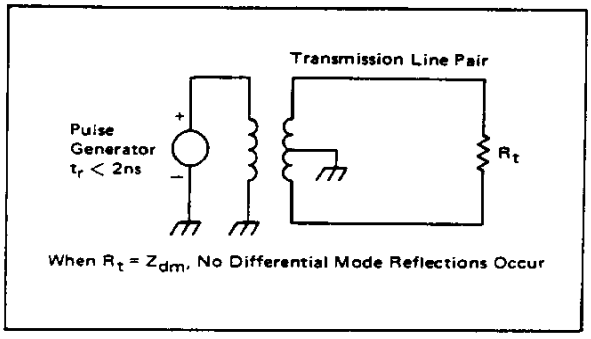

FIGURE 18 – Circuit for Z_{DM} Measurement

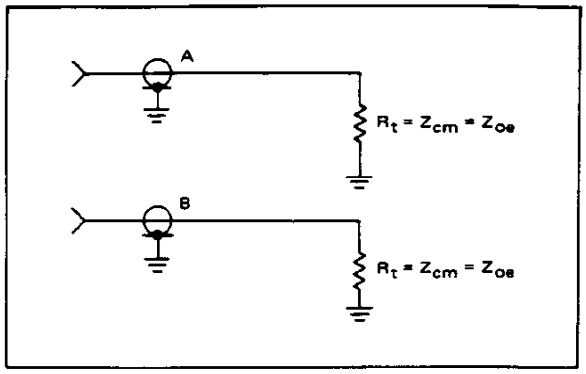

FIGURE 19 – Measuring "Fast Crosstalk"

Figure 18. The pulse transformer is used to assure equal and opposite voltage and current excursions on both lines.

A simpler method of determining the differential mode characteristic is shown in Figure 19. This approach does not require the pulse transformer. Initially, a term called "fast crosstalk", is measured. The measurement technique used (see Figure 19) is to terminate both lines "A" and "B" in Z_{cm} for test will be discussed next. Now, line A is driven and the amount of crosstalk on line B is measured. The following expression can now be used to relate Z_{oe} to Z_{oo}.

$$\frac{\text{Voltage on B}}{\text{Voltage on A}} = \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \qquad (5)$$

or $$Z_{oo} = \frac{V_A - V_B}{V_A + V_B} \times Z_{oe}$$

For example, if the resultant crosstalk is 1 mV for a 10 mV signal on line A, then

$$Z_{oo} = \frac{9}{11} Z_{oe}$$

or $$Z_{dm} = 2Z_{oo} = \frac{18}{11} Z_{oe}$$

The circuit in Figure 20 may be used to measure[10] the value of common-mode characteristic impedance, Z_{cm}. The value of resistors which prevent common-mode reflections is Z_{cm}. When measuring Z_{cm} and Z_{dm} for lines that are part of a cable containing many lines, it is important to terminate the remaining lines in approximately the same way as they will eventually be terminated in a system. This is because the total number of grounded and terminated conductors in the entire cable will affect the value of Z_{cm} and Z_{dm} being measured. Since $2Z_{cm} > Z_{dm}$, it is always possible to choose a delta bridge of resistors that will terminate both the common- and differential-mode signals correctly. The common-mode signal is terminated correctly by a resistor of value Z_{cm} to ground from each line. The differential-mode signal is terminated correctly by a resistor whose value placed in parallel with $2Z_{cm}$ is equal to Z_{dm}. The value of this resistor[10] may be calculated from equation 6 below:

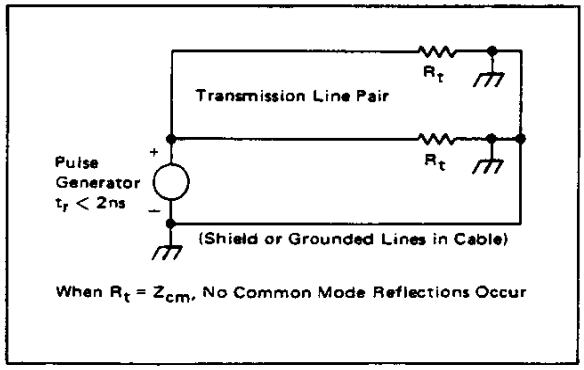

FIGURE 20 – Circuit for Z_{CM} Measurement

$$R_2 = \frac{2(Z_{dm})(Z_{cm})}{2Z_{cm} - Z_{dm}} \qquad (6)$$

Here it should be remembered that Z_{dm} equals twice Z_{oo}.

APPLICATIONS

Applications involving line drivers and receivers may vary from a few feet to thousands of feet. Cables used to transmit the data stream may vary from a simple two-wire twisted pair to a multi-line cable. Thus there are numerous ways to implement a transmission system depending upon the overall system requirements and the discretion of the designer.

This section describes several line driver and receiver examples. The examples shown are categorized into three general areas: differential, single-ended, and duplex applications.

DIFFERENTIAL

This section describes several circuits using TTL or MECL compatible IC's. Since the differential mode is the most popular approach, a brief design analysis is included for one circuit.

Figure 21 uses the MC75110L and MC75107L (line driver and receiver respectively). The transmission line is the same used earlier for the examples under "line considerations". The clock rate is arbitrarily chosen to be 10 MHz.

The attenuation of this line is measured to be 2.6 dB/100 ft. at 10 MHz. The value of $I_{o(on)}$ is typically 12 mA for the MC75110L. The voltage driving one line, defined earlier, is then:

$$V_1 = \frac{I_{o(on)} Z_o}{4}$$

$$V_1 = \frac{(12\text{ mA})(100)}{4}$$

$$V_1 = 300\text{ mV}$$

Thus, the differential input voltage to the cable is 600 mV.

The threshold voltage of the MC75107 is 25 mV. Therefore, a good design value (to offset practical system variables such as termination resistor match, etc.) is 6 dB higher or 50 mV. The allowable cable attenuation (A) is then:

$$A = \frac{600\text{ mV}}{50\text{ mV}} = 12 \text{ or } 21.6\text{ dB}$$

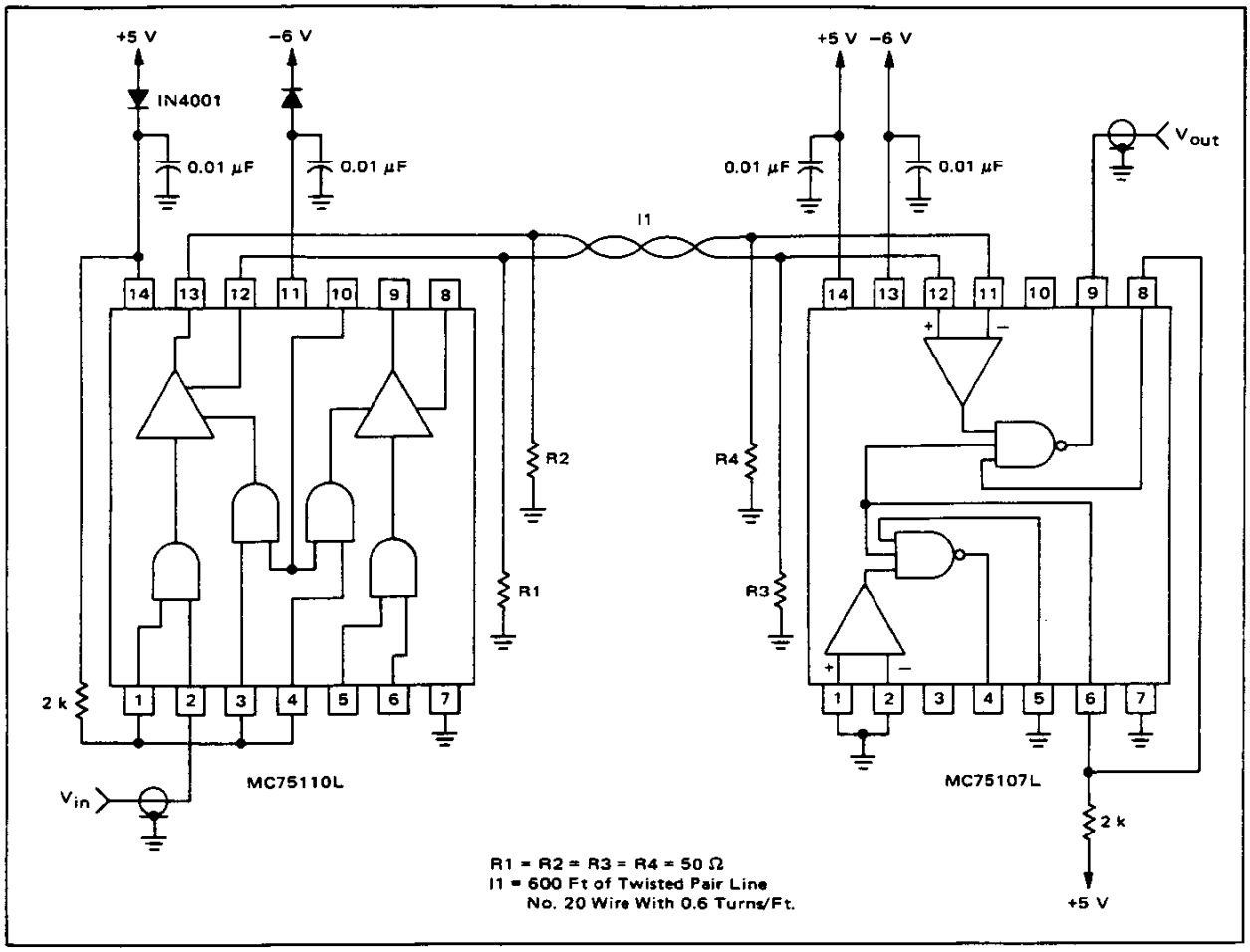

FIGURE 21 – Differential System Using MC75110 and MC75107

The maximum clock rate of the MC75110/MC75107 is typically 10 MHz. However, since it will be shown that a 50% duty cycle is not the limiting case for demonstration purposes, the clock rate is chosen to be 18.5 MHz. For this clock rate, attenuation is approximately 3.53 dB/100 ft. (see Figure 14), and the maximum line length should be:

$$\text{length} = \frac{21.6\ \text{dB}}{3.53\ \text{dB}/100\ \text{ft.}} = 612\ \text{feet}$$

As previously mentioned, a single pulse corresponds to the case where a "1" with a long series of "0's" is being transmitted. For the pull-pull driver used in this example (MC75110L), this means that one line will be at ground and the other line at −300 mV. This negative offset voltage provides an additional restriction on the receiver (MC75107L). Depending on how the line is connected to the receiver, the receiver will either be "on" or "off" until the input signal exceeds approximately 300 mV. For instance, where the 300 mV offset biases the receiver "off", the differential signal to the receiver must be at least 325 mV. This value consists of 300 mV to overcome the offset voltage and 25 mV to overcome the threshold of the receiver. Therefore, for an input differential signal of 600 mV the maximum allowable pulse attenuation is:

$$\frac{325\ \text{mV}}{600\ \text{mV}} = 0.54 \text{ or } 54\%$$

The question now is what is the width of the single pulse that will attenuate this pulse 54%. This problem was solved in the preceding section. The "T_O" of the unshielded twisted pair was calculated to be 109 ns. From Figure 15, it was determined that a pulse width of 136 ns would result in a reduction of the input pulse magnitude by 55%. Therefore, the answer to the question of the maximum pulse width of the single pulse is approximately 136 ns.

If the duty cycle is increased to 50% (while maintaining the 136 ns pulse width) the maximum clock rate (ignoring noise) is:

$$f_{max} = \frac{1}{(2)(136\ \text{ns})}$$

$$= 3.68\ \text{MHz}$$

From this example, it can be seen that the maximum clock frequency is determined by the single-pulse, low duty-cycle condition; the maximum clock frequency with

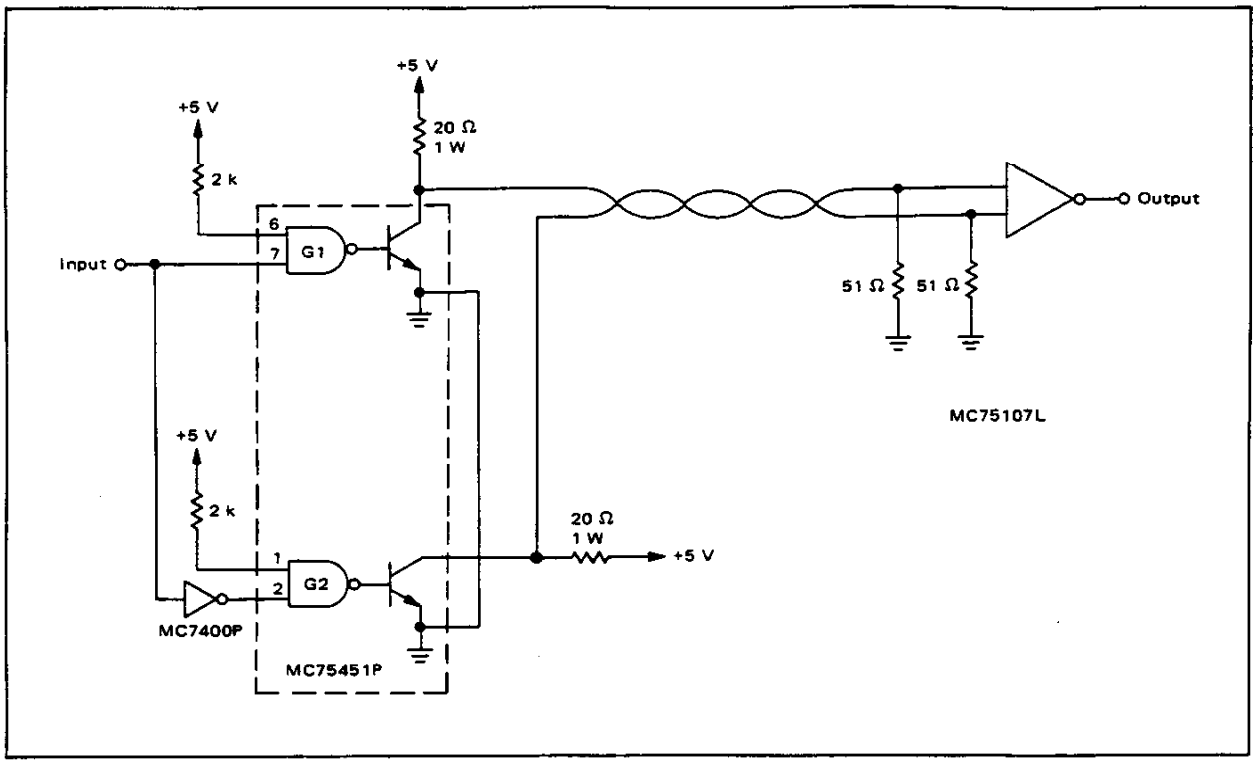

FIGURE 22 – Differential System Using Single Supply Driver

a 50% duty cycle is then 3.68 MHz.

The differential system shown using the MC75110L and MC75107L uses only the two IC's, one line driver, and one receiver. The strobe feature allows these particular IC's to be utilized in party-line or bus applications. For example, if several drivers (MC75110L) are used to drive the line at different times, each can be enabled when desired. In the meantime, the other drivers not in use are disabled. Thus, loading by the unused drivers is held to a minimum.

During party-line operation, it is recommended that each positive and negative power supply feedline to each line driver be fed through a diode (1N4001). Consequently, during power shutdown, a particular driver will not have its outputs pulled below ground (substrate) when another driver pulls the line low.

Figure 22 shows a differential system using the MC75451P and the MC75107L. The MC75451P with a few external components provides a differential signal from a single positive 5 volt supply. The MC75107L requires two supplies. The single external gate shown in Figure 22 provides the required input phase reversal to gate G_2 of the MC75451P. In critical applications, the propagation delay of the MC75400P should be balanced with an equal propagation time through another noninverting gate to G_1 (not shown).

Each output of the MC75451P varies between 0.5 volts and a "high" voltage of approximately 3.6 volts. The net differential voltage driven into the line is approximately 6 volts. It should be noted that only the receiver end of the line is terminated in the characteristic impedance. This is adequate for a point-to-point transmission. Of course, it would not work in a party-line system where an enabled receiver is not necessarily the end of the line.

Figure 23 describes a MECL line driver[1,9] and receiver using gates. This system can be operated from a single supply (as shown in Figure 23). The circuit shown uses MECL levels. If TTL levels are desired, the MC10124 and MC10125 can be substituted for the driver and receiver, respectively. The latter, however, requires an additional negative supply (−5.2 volts).

Figure 24 shows a differential system using the MC3487 and MC3486 line driver and receiver. These IC's are intended primarily for high-speed modem interface (EIA Standard RS422). The termination resistor (R_t) is optional but is recommended to minimize reflections. The value of R_t should equal the characteristic impedance of the line, but in no case should R_t be less than 90 Ω.

The output voltage of the MC3487 is switched from less than 0.5 V to more than 2.5 V which produces a minimum differential signal of 4.0 V. The three-state output of the MC3487 allows multiple drivers on one line in applications where the voltage at the high-impedance output does not exceed 7.0 V or fall below −0.25 volts.

The receiver typically has 50 mV of hysteresis on its input to improve noise immunity and prevent oscillation on the output during the input signal transition. The three-state output makes the receiver bus compatible.

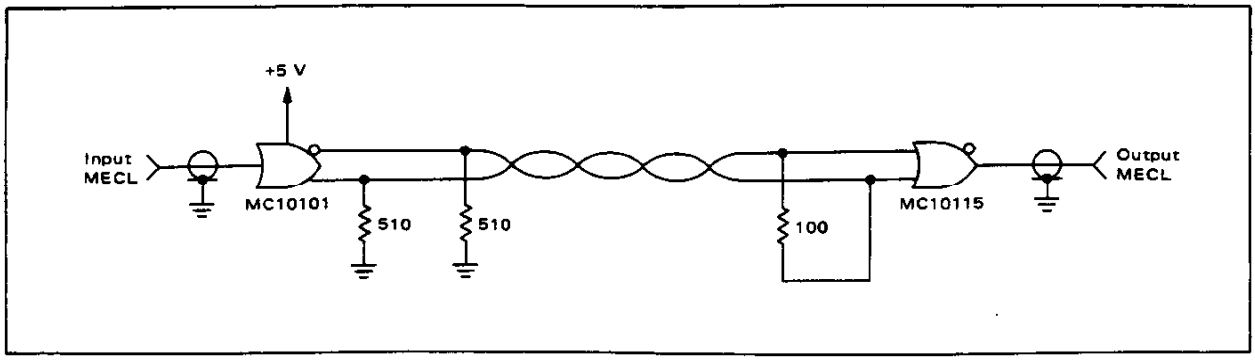

FIGURE 23 – MECL Differential System

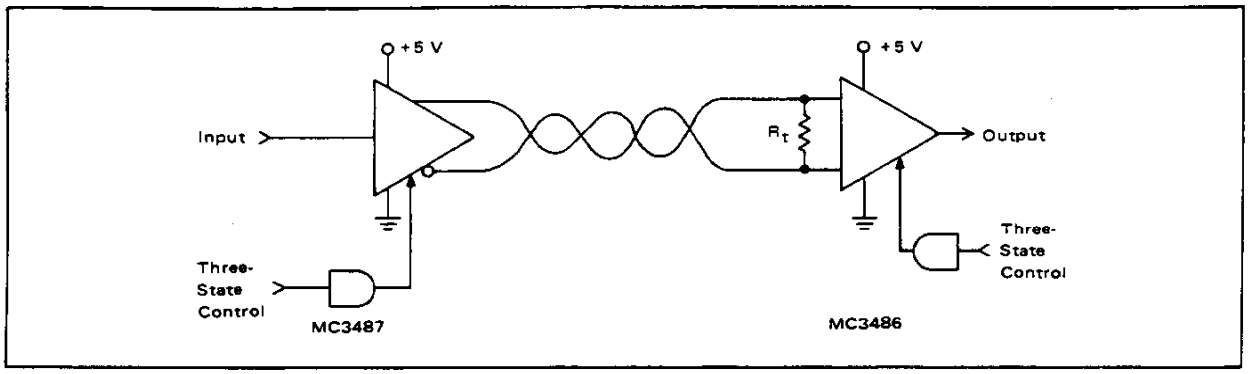

FIGURE 24 – Differential System Using MC3486 and MC3487

SINGLE-ENDED SYSTEMS

Figure 25 describes a point-to-point, single-ended system using a positive supply only. This circuit supplies a 4.2 volt input pulse to the transmission line. Two important considerations here are rise time and dc offset. The frequency for a given length of cable must be small enough to insure adequate "edges" and dc offset for the MC7400P. Excessive offset, as previously explained, results in the receiver always being "on" or "off".

Figure 26 describes a single-ended system using the MC1488 and MC1489 line driver and receiver, respectively. These IC's are intended primarily as modem interfacing devices (EIA Specification RS-232C). Both the driver and receiver are flexible in terms of use with regard to DTL, TTL, MOS and MECL logic levels. The system utilized in Figure 26 is intended for an input and output data stream using TTL. The typical operating frequency is 2 MHz.

Figure 27 shows an unbalanced system using the MC3488 and MC3486 line driver and receiver. These IC's are also intended as modem interface devices (EIA Standard RS423).

Output waveshaping is employed to control the interference (near-end crosstalk) that may be coupled to adjacent circuits in the interconnection. The rise time of the driver output is controlled by the wave-shaping resistor (R_W). The rise time is defined as the time it takes for the output waveform to rise from 10% to 90% of its final value. Figure 28 shows the signal wave-shaping requirement for RS423 compatible systems. Figure 29 shows the output rise time of the MC3488 as a function of the wave-shaping resistance.

Since the driver's output is slew rate limited, a termination resistor is not normally used. If the line is terminated, the equivalent input resistance between the input points (A and B, Figure 27) must be more than 400 Ω.

DUPLEX SYSTEMS

The MC10194 Dual Simultaneous Bus Driver/Receiver is designed for high-speed data transfer over multi-port bus lines. Full duplex data transmission can improve system performance by increasing message density and overcoming the requirement to wait two line propagation delay times between messages.

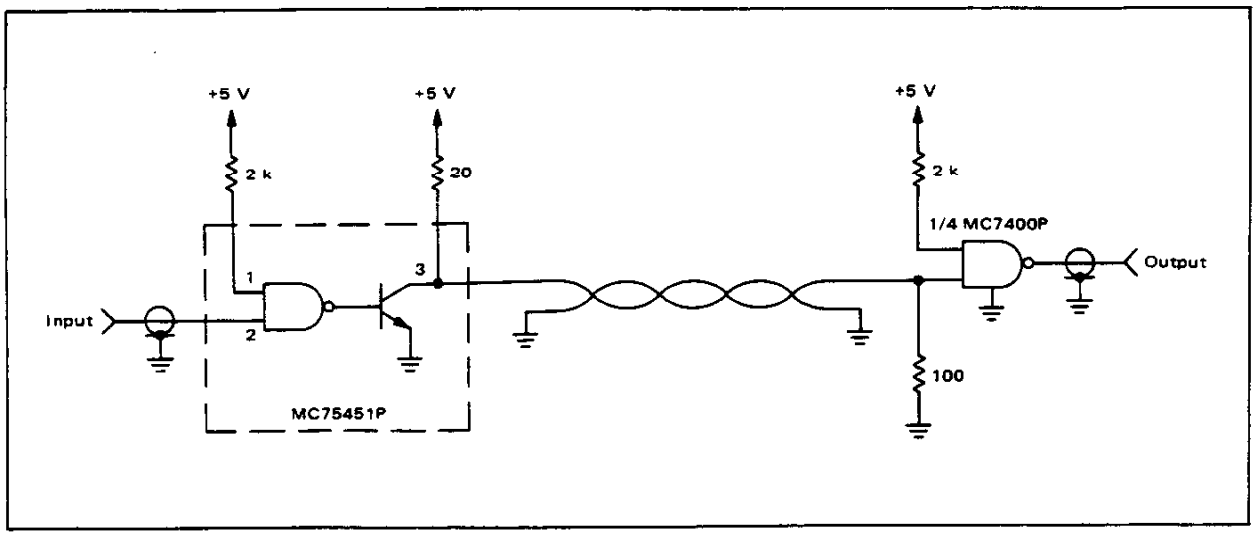

FIGURE 25 – Single-Ended, Single Supply

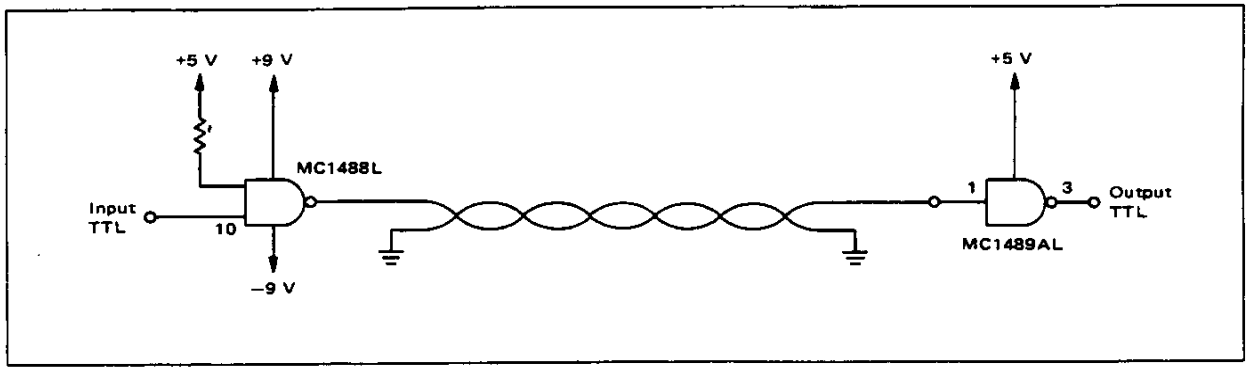

FIGURE 26 – Single-Ended System Using MC1488L and MC1489AL

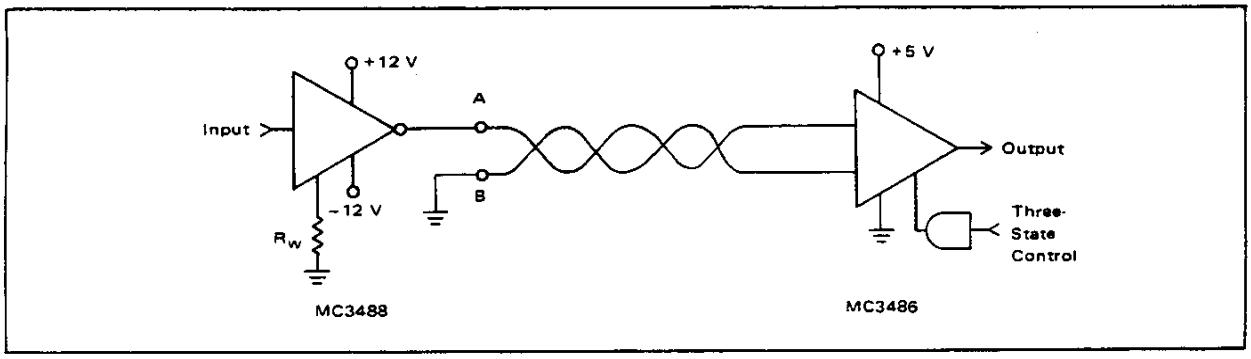

FIGURE 27 – Unbalanced System Using MC3488 and MC3486

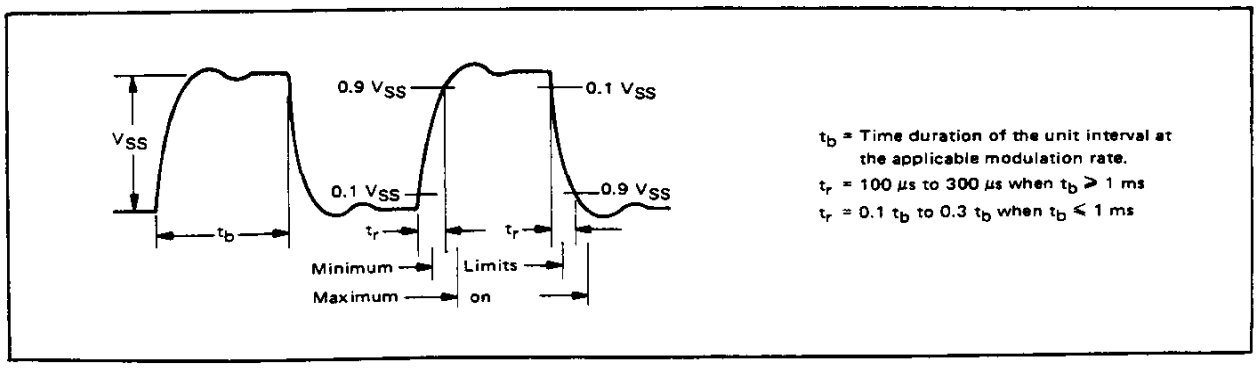

FIGURE 28 – RS423 Signal Wave-Shaping Requirement

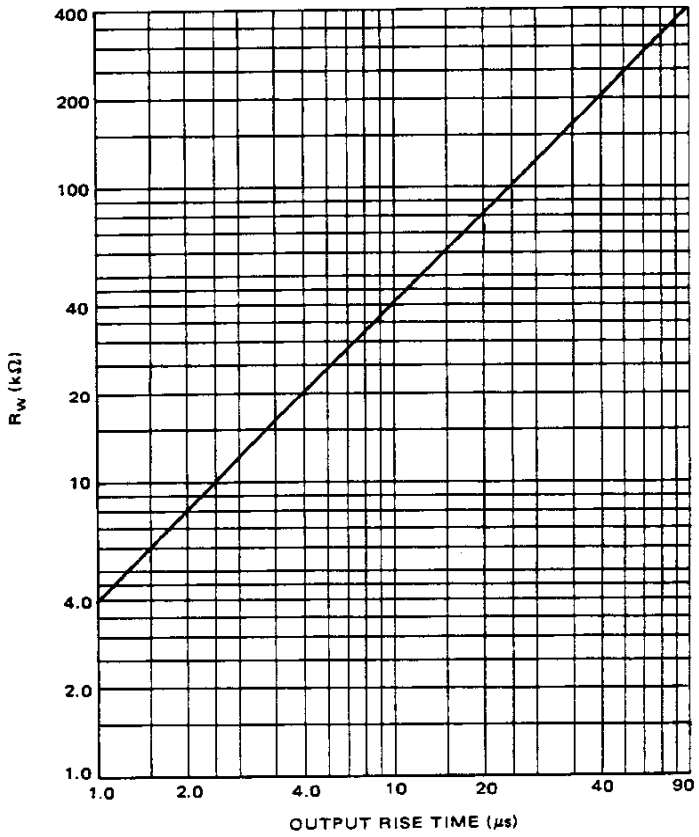

FIGURE 29 – MC3488 Wave-Shaping Control

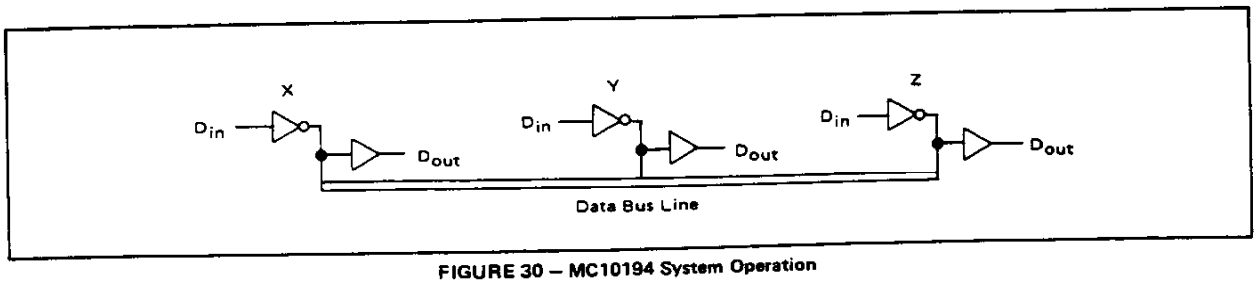

FIGURE 30 – MC10194 System Operation

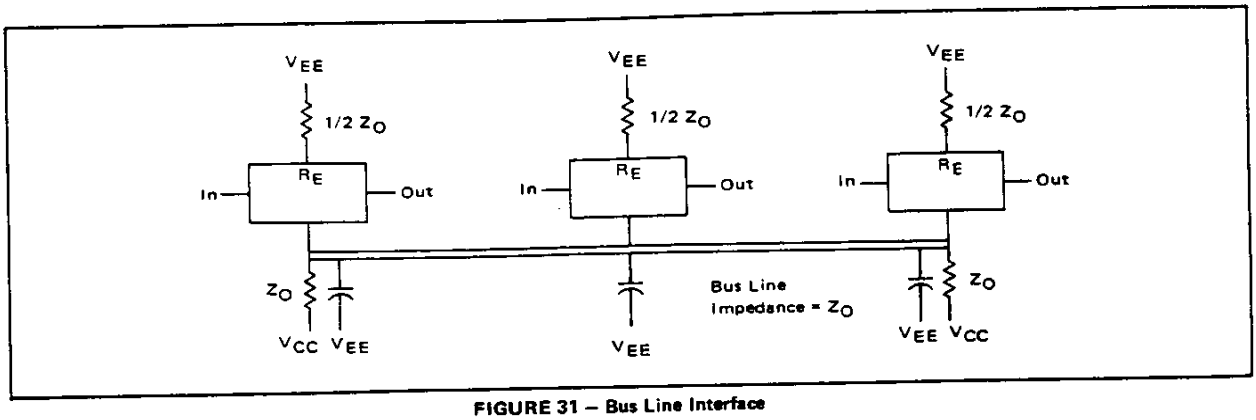

FIGURE 31 – Bus Line Interface

Figure 30 illustrates system uses for the MC10194. One mode of operation is with two drivers on the bus line at locations X and Z. Any input to D_{in} X is seen at D_{out} Z one line propagation delay later. Similarly, any input to D_{in} Z is transmitted to D_{out} X. Each driver inhibits the data being sent on the bus from appearing at its receiver output, so full duplex signal transmission is possible. In addition, current source drivers allow two messages to pass on the same line so there are no timing restrictions between sending messages.

A second type of system operation is with a multi-terminal bus as illustrated in Figure 30 by points X, Y, and Z. In this mode, any one terminal can transmit data and all other points will receive the message. Alternately, any two terminals can simultaneously exchange data, but the other receivers will not see valid data.

The MC10194 is a MECL 10,000 series device and uses current source line driving and is designed to operate with a load to V_{CC} (normally ground) when operated from a −5.2 volt supply. This load is usually the line termination resistors at each end of the line as shown in Figure 31. In addition, to match the driver to a given impedance line, an external resistor equal to one-half the line termination resistor value is connected between the R_E output and V_{EE}. When the circuit is used with a multi-terminal bus, each driver must have the resistor between R_E and V_{EE}, but the termination resistors are required only at each end of the bus line.

Each MC10194 driver in a package is capable of driving 75-ohm lines. Higher impedance lines may be used with no loss of performance if the line is properly matched with R_E. If it is desirable to drive 50-ohm lines, both drivers in a package should be operated in parallel with each having 50-ohm resistors at R_E and the driver outputs both connected to the 50-ohm bus lines.

To allow very high data rates, the rise and fall times on the bus line are quite fast (typically 1.0 ns). With full duplex operation, it is possible to get a crosstalk pulse of several hundred mV at a receiver output. A 10–20 pF capacitor connected between each driver output and V_{EE} will slow down the rise and fall times, greatly reduce any crosstalk pulse, and still give good system performance.

The adjustable current source drive feature of the MC10194 makes this circuit a useful output driver for many applications. For example, it is possible to drive the 50-ohm to ground load required by many interface systems. This driver will sink the 14 to 18 mA required to meet the AEC Committee specification for Nuclear Instrumentation Modules. The MC10114 MECL Line Receiver makes a good interface receiver for the MC10194 driver in these applications.[14]

PRODUCT SELECTION

The actual selection of the line driver and receiver will depend on many factors including cost, power supply voltages, logic level, clock rate, length of line, etc. Available Motorola line drivers and receivers are summarized in Figures 32 through 37. More detailed specifications for these devices can be found in the individual product data sheets.

CONCLUSION

This report discusses many of the design considerations relevant to line drivers and receivers. Emphasis was placed

Functional Description	Logic Compatibility	Output Current ON mA Typ.	Output Current OFF μA Max.	Prop. Delay Input to Output ns Typ.	Prop. Delay Inhibit to Output ns Typ.	Device Number
Dual Driver with Inhibit Inputs	MTTL	12 mA	100	9.0	16	MC75110
Quad Driver with Strobe	MTTL	11 mA	100	9.0	18	MC3453A
Quad Driver, Single-Ended	MDTL/MTTL	Conforms to EIA Specification RS-232C.				MC1488
Quad Driver, Differential	MDTL/MTTL	Conforms to EIA Specification RS-422				MC3487
Quad Driver, Single-Ended	MDTL/MTTL	Conforms to EIA Specification RS-423				MC3488

FIGURE 32 – TTL Compatible Line Drivers

Functional Description	Logic Compatibility	Output Current ON mA	Prop. Delay Input to Output ns Typ.	Device Number
Dual NAND Driver with Non-Connected Output Transistors	MTTL	300	21	MC75450
Dual NAND Driver	MTTL	300	71	MC75451
Dual AND Driver	MTTL	300	18	MC75452
Dual NOR Driver	MTTL	300	17	MC75453
Dual OR Driver	MTTL	300	25	MC75454

FIGURE 33 – TTL Compatible Peripheral Drivers

Functional Description	Logic Compatibility	Input Threshold mV Max	Input Common Mode Range V Min	Prop. Delay Input to Output ns Typ	Prop. Delay Input to Output ns Typ	Device Number
Dual Line Receiver with Active Pull-Up	MTTL	± 25 mV	± 3 V	18	10	MC75107
Dual Line Receiver with Open Collector Output	MTTL	± 25 mV	± 3 V	19	13	MC75108
Quad Line Receiver with Active Pull-Up (Tri-State Strobe)	MTTL	± 25 mV	± 3 V	25	10	MC3450
Quad Line Receiver with Open Collector Output	MTTL	± 25 mV	± 3 V	25	13	MC3452
Quad Receiver, (RS-232C) Single-Ended	MDTL/MTTL	–	–	120	–	MC1489, A
Dual Line Receiver Single-Ended	MTTL	± 100 mV	–	22	10	MC75140
Quad Receiver (RS-422, RS-423) Differential	MDTL/MTTL	± 200 mV	± 7 V	20	25	MC3486

FIGURE 34 – TTL Compatible Line Receivers

Single Ended	Propagation Delay	Gate Power	Edge Speed	Typical Frequency Capability
10,000 Series (All Outputs)	2.0 ns	25 mW	3.5 ns	150 MHz
10123 Bus Driver	2.0 ns	25 mW	3.5 ns	150 MHz
MECL III (All Outputs)	1.0 ns	6.0 mW	1.0 ns	350 MHz
Differential				
10 K Series	2.0 ns	25 mW	3.5 ns	150 MHz
MECL III	1.0 ns	60 mW	1.0 ns	350 MHz
MC10124 Quad TTL-MECL Translator	5.0 ns	85 mW	2.5 ns	75 MHz

FIGURE 35 – MECL Compatible Line Drivers

Single Ended	Propagation Delay	Gate Power	Edge Speed	Typical Frequency Capability	Common Mode
10,000 Series (All Inputs)*	2.0 ns	25 mW	3.5 ns	150 MHz	–
MECL III (All Inputs)*	1.0 ns	60 mW	1.0 ns	350 MHz	–
Differential					
MC10114	2.0 ns	25 mW	3.5 ns	100 MHz	±1 V
MC10115, Quad	2.0 ns	25 mW	3.5 ns	125 MHz	+0.7 V, −1.5 V
MC10116, Triple	2.0 ns	25 mW	3.5 ns	125 MHz	+0.7 V, −1.5 V
MC10216, Triple	1.2 ns	25 mW	2.5 ns	150 MHz	+0.7 V, −1.5 V
MC1692	1.0 ns	60 mW	1.0 ns	325 MHz	+0.7 V, −1.0 V
MC10125, Quad MECL-TTL Translator	5.0 ns	90 mW	2.5 ns	75 MHz	±2.5 V

*NOTE: Input impedance is typically 50 kΩ shunted with 3.5 pF.

FIGURE 36 – MECL Compatible Line Receivers

	Propagation Delay (Typ)	Output Rise and Fall Time	Typical Frequency Capability	Features	Device Number
Dual MECL Bus Transceiver	2.5 ns	2 ns	100 MHz	Adjustable Current Drive to 50 Ω	MC10194
Dual Interface Line Driver/Receiver	500 ns	–	500 kHz	Adjustable Hysteresis, CMOS and MHTL Compatible	MC696

FIGURE 37 – Duplex Transceivers

on subject material such as system description, definition of terms, design procedures, and application examples. More extensive and detailed information was supplied in numerous references.

Copies of EIA Standards mentioned may be obtained for a small fee by writing to:

Electronic Industries Association
Engineering Department
2001 Eye Street, N.W.
Washington, D.C. 20006

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