

APPLICATION NOTE

AN251 AVC Logic Family

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AVC Logic Family

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INTRODUCTION

Philips Semiconductors has introduced a new low voltage logic family optimized for high performance bus interface applications: AVC (Advanced Very low voltage CMOS). Operating with sub 2 ns propagation delays, AVC meets the demands of new digital systems that require low power consumption, very high bus speeds in excess of 100 MHz, and low noise. AVC is targeted for new high performance workstations, PCs, telecommunications equipment, and data communications equipment.

New circuit techniques have been pioneered that give AVC unique properties. Optimized for 2.5V systems, AVC also operates at 3.3V and 1.8V to support mixed voltage systems. Dynamic Controlled Outputs, DCO™, allow high switching speeds while changing the output impedance to reduce transmission line reflections. This eliminates the need for external series terminating resistors. AVC also features a power-off disable output circuit that isolates the outputs during power-down modes. This paper will provide designers better insight into this new family for use in their applications.

BASIC PROPERTIES OF AVC

AVC is fabricated on a 0.35 micron advanced CMOS process that enables very short propagation delays while maintaining low power dissipation. Some basic properties are shown in Table 1:

Table 1. Basic AVC Characteristics

PARAMETER	CHARACTERISTIC VALUES		
	1.65 – 1.95V	2.3 – 2.7V	3.0 – 3.6 V
Supply voltage	1.65 – 1.95V	2.3 – 2.7V	3.0 – 3.6 V
Input voltage	3.6 V	3.6 V	3.6 V
V _{IH}	0.65V _{CC}	1.7V _{CC}	2.0V _{CC}
V _{IL}	0.35V _{CC}	0.7V _{CC}	0.8V _{CC}
DC I _{OL} /I _{OH} current ¹	±4 mA	±8 mA	±12 mA
Quiescent current	20 µA	20 µA	40 µA
Maximum propagation delay ²	3.2 ns	1.9 ns	1.7 ns

NOTES:

1. DCO™ circuit provides higher dynamic current needed during output transitions.
2. 74AVC16245

INTERNAL CIRCUITRY AND FEATURES

Input Structures

AVC inputs use a CMOS totem pole inverter as shown in Figure 1. The circuit does not have the overshoot clamping diode from the input to V_{CC} that is used in classic CMOS circuits. Since there is no current path to V_{CC}, the voltage may be raised above the V_{CC} level and allows interfacing in 1.8 V to 3.3 V systems.

Since the circuit is CMOS, care must still be taken to ensure that the inputs don't float. When inputs float, the voltage level may reach the threshold level such that both transistors in the totem pole structure will conduct, causing a current path from V_{CC} and ground, wasting power.

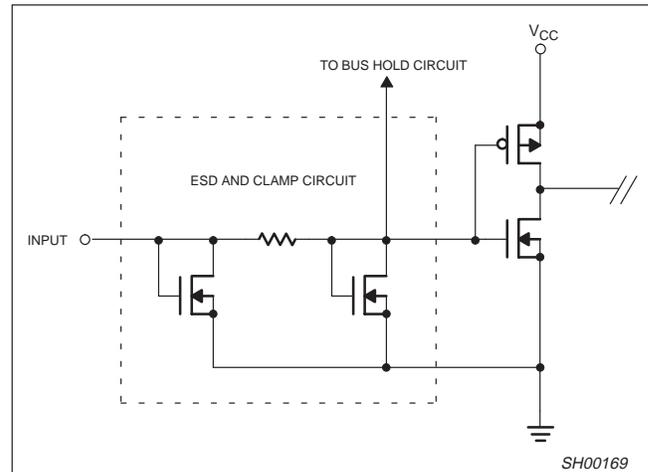


Figure 1. Simplified AVC input structure

Also, floating inputs can cause output oscillation, creating excessive current and heat which can damage the device. To keep inputs from floating, a common practice is to tie a pull-up resistor of several thousand ohms between the input and V_{CC}. Although effective, this adds board component count and extra power dissipation. Another solution is to use a device with an integrated bus hold cell. AVC devices have an option to integrate this bus hold feature on inputs. This is designated in the part type with an "H" by calling it 74AVCH. Figure 2 shows a bus hold cell:

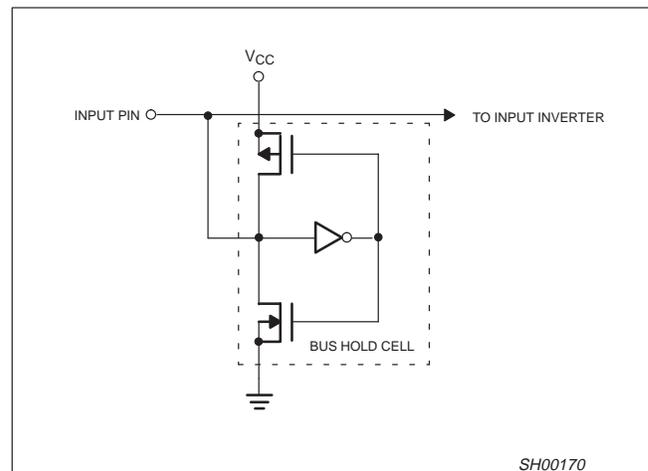


Figure 2. Simplified bus hold cell

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The cell consists of two inverters to keep the logic level the same at the input node. The inverters are comprised of small MOS transistors with weak drive capability in the order of several hundred microamps. When the input starts to float, the PMOS or NMOS structures pull the bus to the V_{CC} or ground rail of the last valid logic state. The cell requires a small amount of current, called I_{BHH} or I_{BHL} , to sustain the logic HIGH and LOW threshold levels. Also, the cell needs several hundred microamps, called I_{BHLO} or I_{BHLO} , to overdrive the cell and flip the logic level from 3-State to a HIGH or

LOW. These specifications are shown in Table 2. Simulation data for the bus hold current characteristics are shown in Figure 3.

The user must also take considerations when the bus hold cell is connected to existing external pull-up or pull-down resistors. When using external resistors, or when a connected ASIC has them built-in, the resistor value must be low enough to allow sufficient current to overpower the bus hold cell and drive the input past the threshold point to the HIGH or LOW state.

Table 2. Bus hold current specifications

SYMBOL	PARAMETER	$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}$ MIN	UNIT	TEST CONDITIONS	
			UNIT	$V_{CC} \text{ (V)}$	$V_I \text{ (V)}$
I_{BHL}	Bus hold LOW sustaining current	25	μA	1.65	$0.35V_{CC}$
		45	μA	2.3	0.7
		75	μA	3.0	0.8
I_{BHH}	Bus hold HIGH sustaining current	-25	μA	1.65	$0.65V_{CC}$
		-45	μA	2.3	1.7
		-75	μA	3.0	2.0
I_{BHLO}	Bus hold LOW overdrive current	200	μA	1.95	
		300	μA	2.7	
		450	μA	3.6	
I_{BHHO}	Bus hold HIGH overdrive current	-200	μA	1.95	
		-300	μA	2.7	
		-450	μA	3.6	

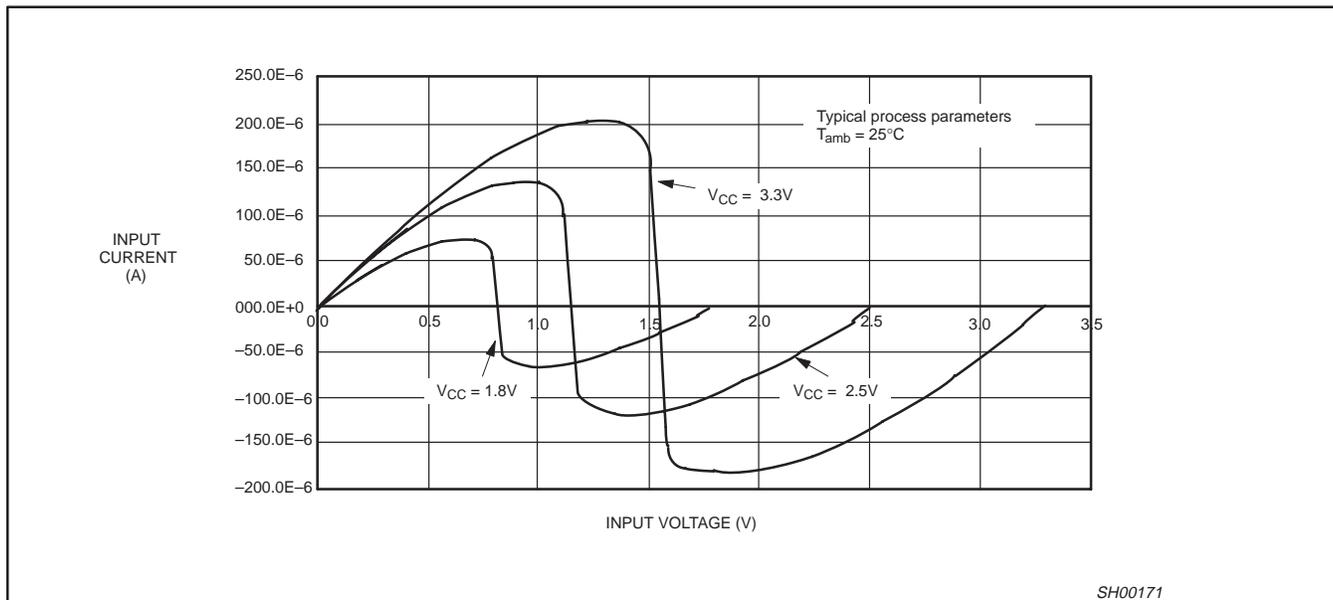


Figure 3. Bus hold current characteristics

DCO™ Output Circuit

A key feature of the AVC family is its innovative output circuit called, Dynamic Controlled Output, DCO™. The DCO™ circuit changes the output impedance and drive current during the signal transition. Static drive currents are low and specified from 4–12 mA to maintain DC V_{OH} and V_{OL} levels, however, current is greatly increased during output transitions. This results in fast signal transitions with minimal overshoots and undershoots. Figure 4 illustrates an output transition.

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The waveform is divided into several regions to show the effects of changing output impedance and drive current. Region A shows the steady state level where drive current is low and impedance is high. In Region B, the impedance is lowered, and drive current is increased to drive the load. In Region C, the impedance is increased, drive current is lowered, and the signal settles towards a steady state HIGH. The increased output impedance has the same effect as adding output termination resistance to dampen reflections. The changes in output impedance and drive current can be better understood by examining the output curves for current versus voltage.

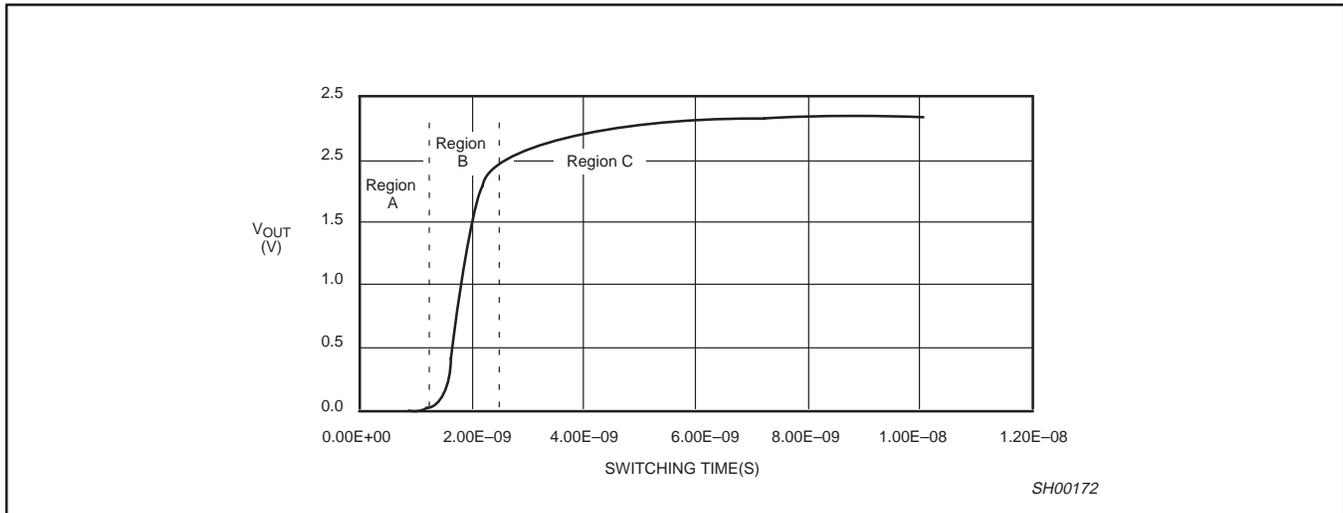


Figure 4. DCO™ waveshape

Figure 5 shows I_{OL} sink current available at various levels of V_{OL} . Using the 2.5 V V_{CC} curve as an example, the slope of V versus I along the curve determines the impedance. The impedance can also be calculated at any point along the curve at the V/I intersect point. When V_{OL} is steady state around the 0 V level, the equivalent output impedance is about 40 Ω , and the drive current is very low. When the output starts to transition from LOW to HIGH, the I_{OH} and V_{OH} curves in Figure 6 can be used.

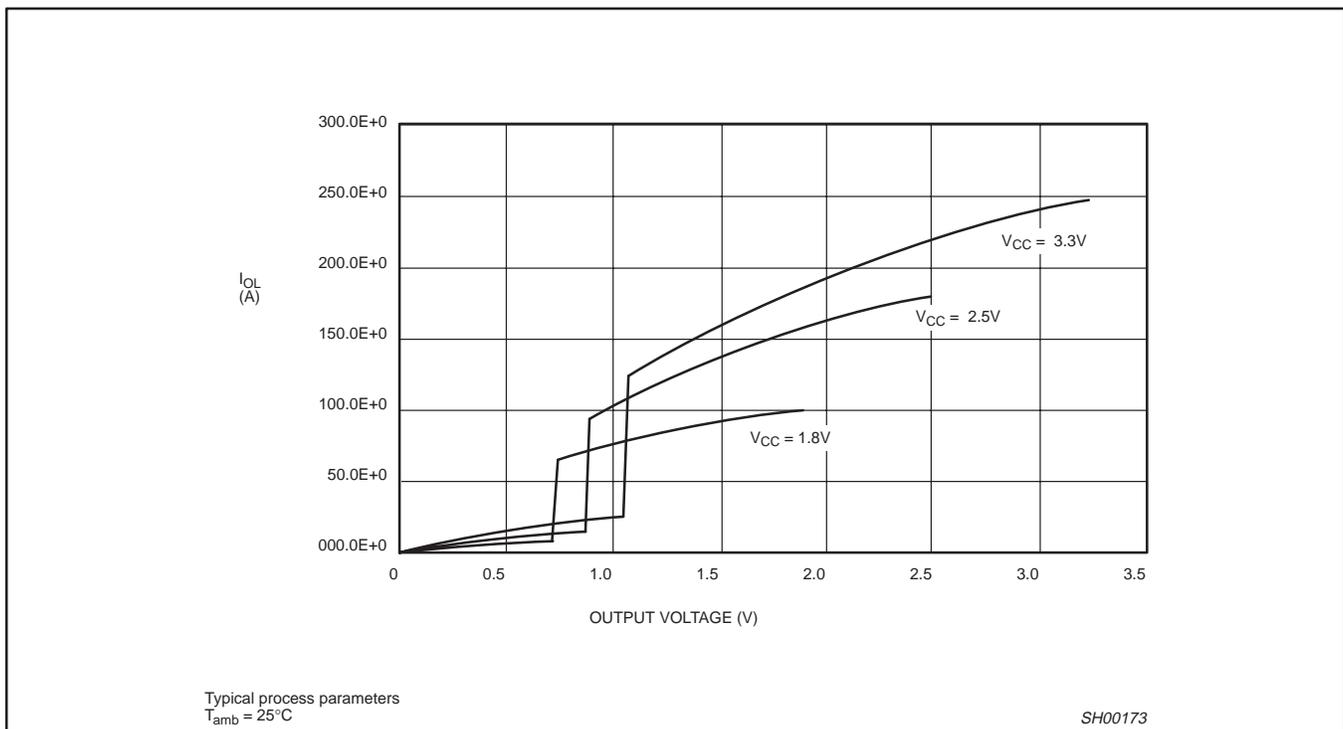


Figure 5. I_{OL} vs. V_{OL}

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Note that there are two impedance regions in the curve. When the signal changes from LOW to HIGH, the initial impedance is about $22\ \Omega$ around the $0\ \text{V}$ region of the curve. The higher drive current is available to drive the load. As the voltage transitions past a $1.25\ \text{V}$ threshold region and settles toward V_{OH} , current is greatly reduced, and the slope of the I/V curve changes. In this region the impedance is around $45\ \Omega$, and the drive current is low.

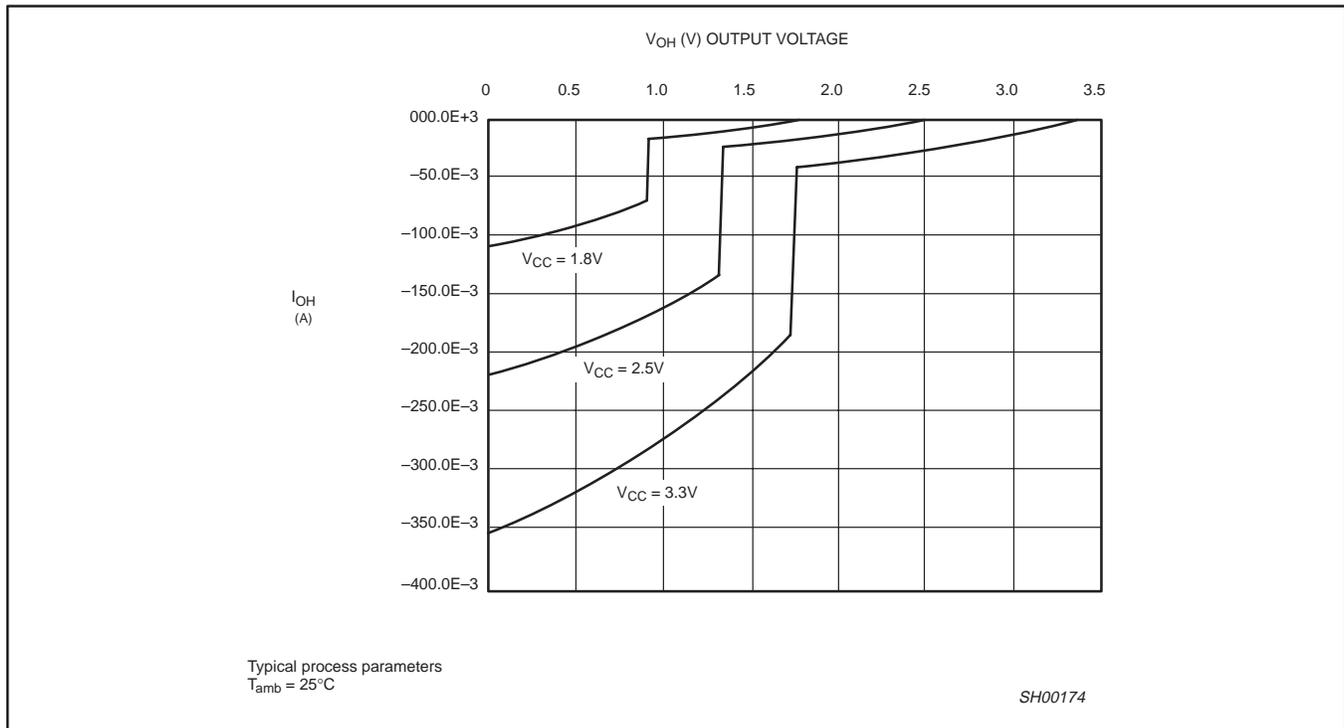


Figure 6. I_{OH} vs. V_{OH}

When the signal changes from a HIGH to a LOW state, the output characteristics are similar. To determine the changes to drive current and impedance, the same methods can be applied by starting with the I_{OH} and V_{OH} curves of Figure 6. At the $2.5\ \text{V}$ steady state condition, the impedance in that region is about $45\ \Omega$. In Figure 5 note that the curve also has two regions with different slopes. Going from a HIGH to a LOW, the impedance starts out around $23\ \Omega$ with high drive current and goes past a $0.9\ \text{V}$ threshold region. After the threshold, current drops and the impedance increases to $40\ \Omega$ as the signal settles to a steady state V_{OL} level.

Figure 7 shows the DCO™ output circuitry. The output stage consists of PMOS (P1 and P2) and NMOS (N1 and N2) transistors in totem pole configurations. N1 or N2 provide I_{OL} sink current to pull down the output node to the a LOW level while the P1 or P2 provide I_{OH} source current to pull up the output node to a logic HIGH level. The drains of all four transistors are common. P1 and N1 form one totem pole while P2 and N2 form the other totem pole. The two totem poles are dynamically connected in tandem through their gate nodes by the control circuitry. The connection of these totem poles produces changing output impedances and changing drive currents as the output signal transitions.

When the output voltage is at a steady state V_{OH} or V_{OL} level, P1 or N1 is driving the output. During this static condition, the single transistor produces an output impedance of about $40\ \Omega$ in the LOW state and $45\ \Omega$ in the HIGH state when V_{CC} is $2.5\ \text{V}$. The control circuit is also monitoring the output voltage level. When the driver starts to transition from one logic level to the other, the control circuit connects both totem poles. Drive current is increased, and the output impedance drops to about $22\ \Omega$.

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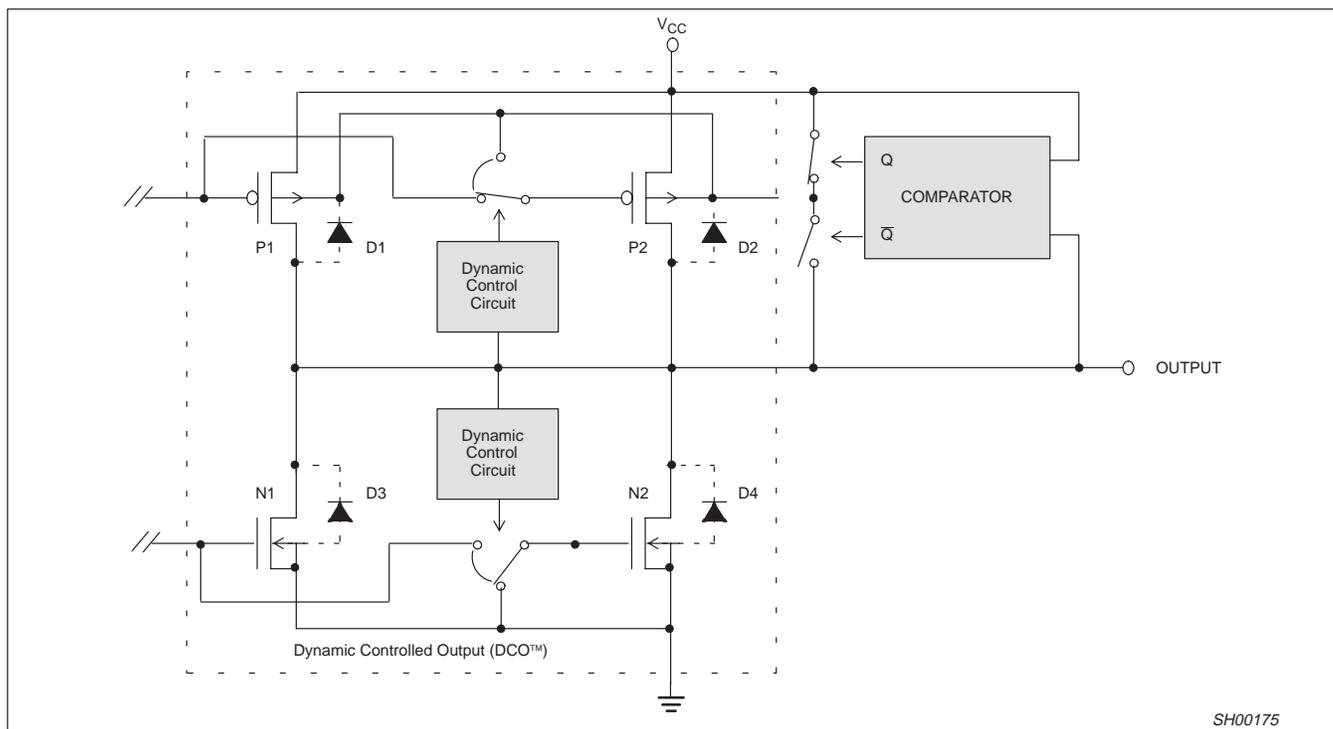


Figure 7. Simplified DCO™ output structure

When the signal edge transitions past the 1.25 V threshold going from LOW to HIGH or goes past the 0.9 V threshold while going from HIGH to LOW, the control circuit disconnects the totem poles. Now only P1 or N1 is on, drive current is reduced, and equivalent output impedance increases back to the 40–45 Ω range.

Figure 4 illustrated the behavior of an unterminated DCO™ signal. To achieve the same level of signal integrity from a more conventional high performance device, such as ALVC, termination resistance must be added. If a series damping resistor is used, it will reduce drive current and signal speed which may be undesirable. By using AVC with its innovative DCO™ circuitry, the dynamic output impedance adds resistance when needed to dampen reflections, and fast switching speeds are maintained.

Based on the switching characteristics of the DCO™ output, line termination is generally unnecessary. End termination with resistors is not recommended since the resulting DC current can exceed the DC static sink and source current ratings. AVC devices are suitable for single point or distributed load applications, such as memory drivers and registers.

Output Protection

Another feature of AVC is the output protection circuit. The purpose of the comparator in Figure 7 is to protect the CMOS parasitic diodes, D1 and D2, normally connected between the drain and V_{CC} . In mixed voltage systems, when the output node is tied to a bus from a higher voltage system, the original diode connection provides a current path to V_{CC} when the output node is 0.6 V higher than the AVC device's V_{CC} . This current can damage the diode, and a current path now exists between the two power supplies. Damage can also occur from the higher voltage supply charging the lower voltage supply.

To protect the diodes, the cathodes are switched rather than hard-wired to V_{CC} . The comparator senses the output node voltage and shorts out the diode when the voltage rises above the AVC device's V_{CC} by 0.6 V. This works in the 3-State mode only, and the current path to V_{CC} is eliminated, allowing the output to be raised above V_{CC} in a mixed voltage system.

While the device is powered down, the diodes are disconnected, and only leakage current of 10 μA maximum is present when a voltage is applied to the output. This current parameter is called I_{OFF} , and the protection feature is useful for power-down modes.

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DEVICE CHARACTERISTICS

Power Dissipation

AVC is constructed using an advanced 0.35 micron CMOS fabrication process resulting in low current consumption. Figure 8 shows simulation data of I_{CC} at various frequencies for single and multiple output switching:

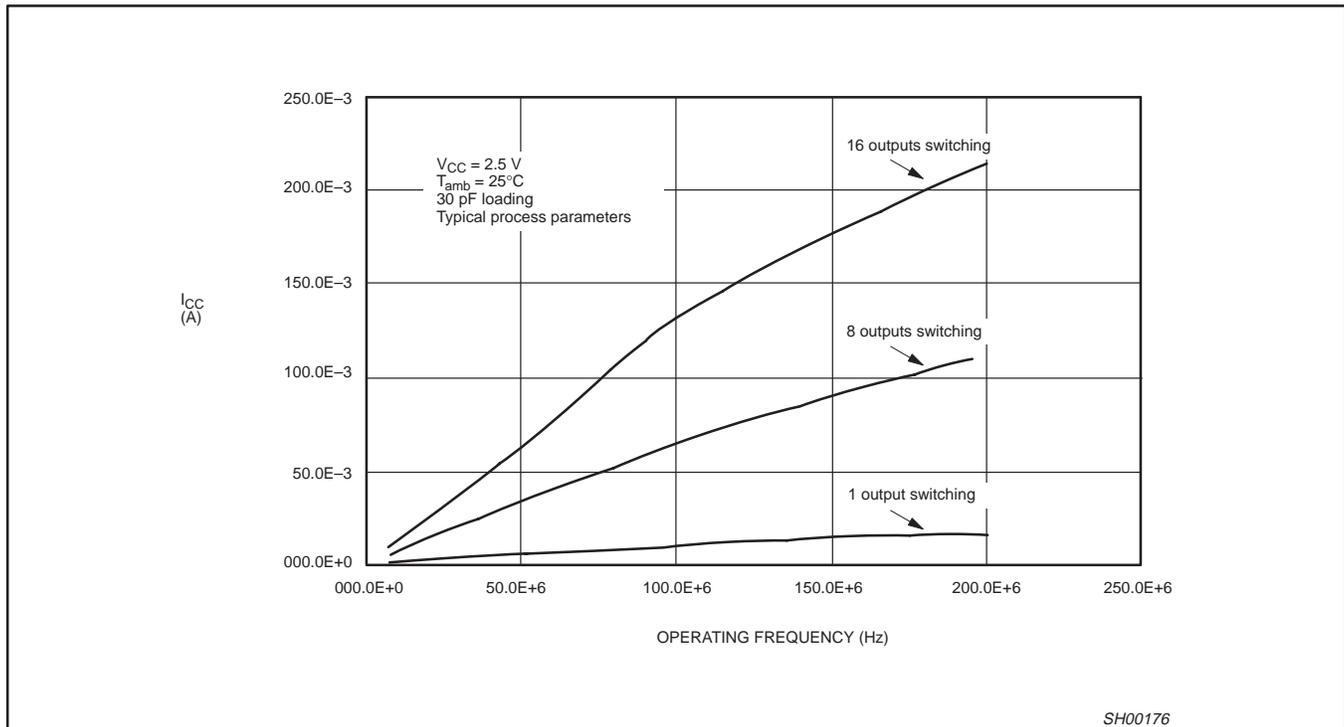


Figure 8. I_{CC} vs. frequency

Dynamic power dissipation can be calculated by the following formula:

$$P_D = C_{PD} \times V_{CC}^2 \times f_{IN} + \Sigma(C_L \times V_{CC}^2 \times f_{OUT})$$

where: C_{PD} = power dissipation capacitance per buffer, latch, or flip-flop

f_{IN} = input frequency

f_{OUT} = output frequency

C_L = output load capacitance

$\Sigma(C_L \times V_{CC}^2 \times f_{OUT})$ = sum of outputs

For an example, with a typical C_{PD} of 20 pF for an AVC16244, 15 pF loading, 100 MHz operation, and 2.5 V V_{CC} , power dissipation is 162.5 mW with 16 outputs switching.

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Ground Bounce

High-speed parts typically exhibit more ground bounce than slower parts where speed and ground bounce are a tradeoff. AVC is designed to optimize the performance of propagation delays and ground bounce. The family is offered in the TSSOP package in 48 and 56 pin counts. The package features multiple V_{CC} and ground pins to reduce the effective ground and V_{CC} pin inductance that contributes to ground and V_{CC} bounce. Figures 9 and 10 show simulation data for these parameters.

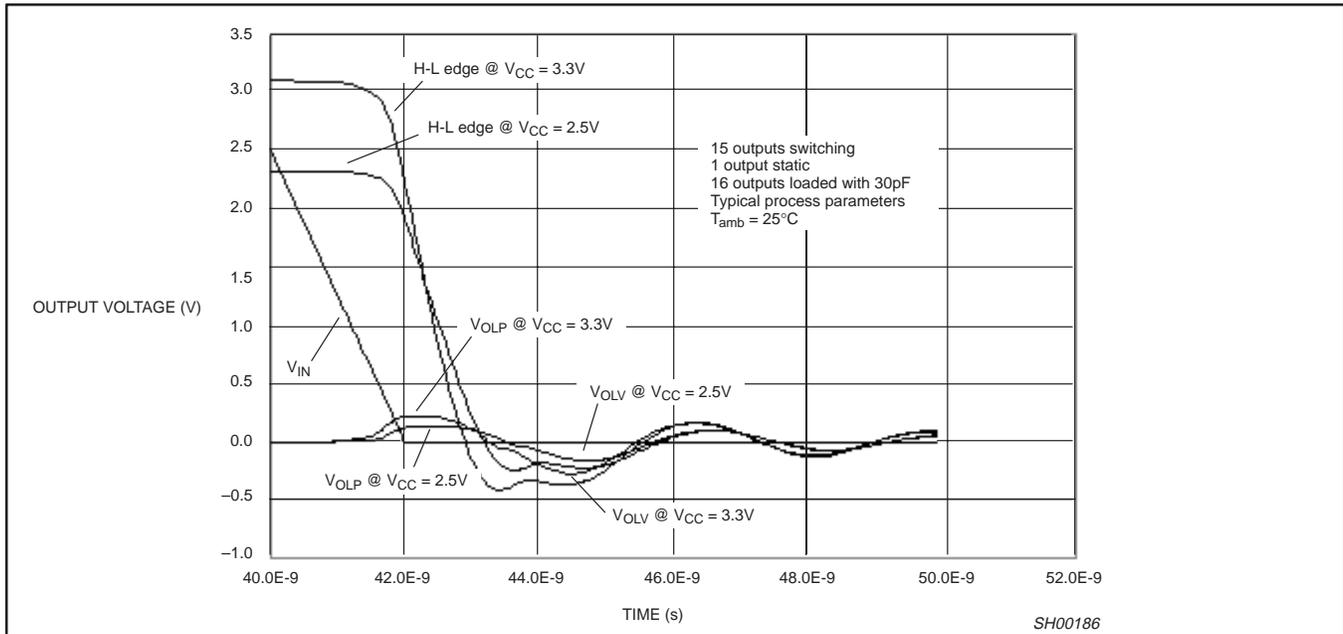


Figure 9. Ground bounce waveforms

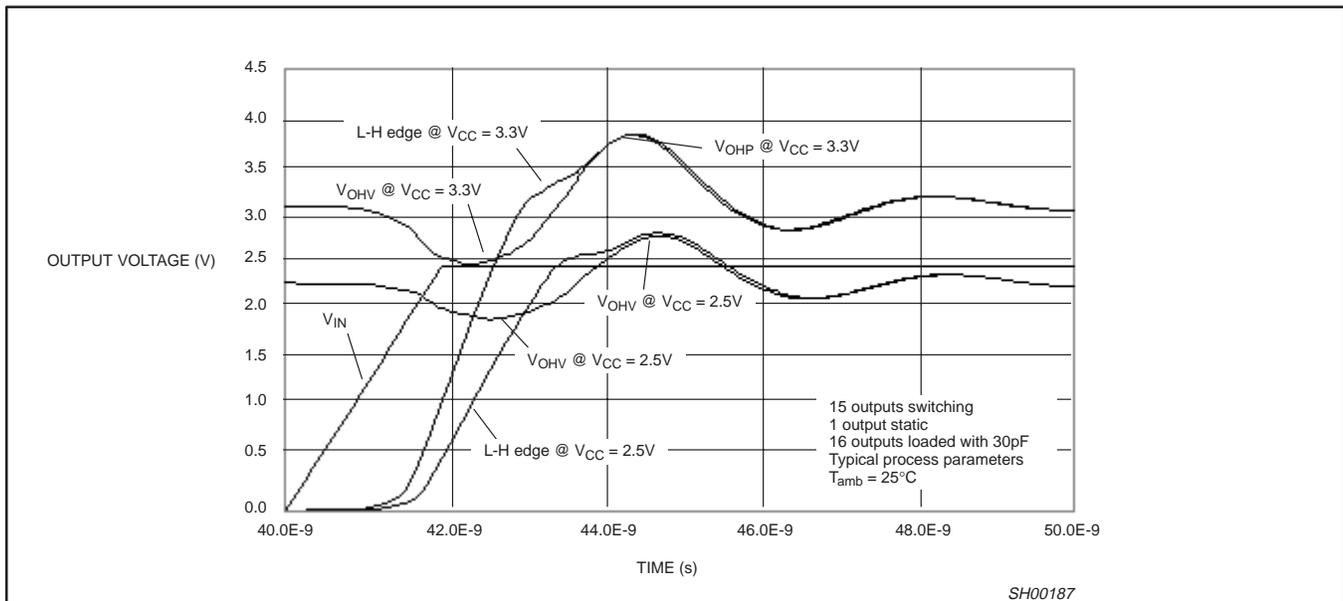


Figure 10. VCC bounce waveforms

The combination of low voltage swings, reduced package inductance, and advanced output circuitry results in excellent ground and V_{CC} bounce performance as observed in the V_{OLP} , V_{OLV} , V_{OHV} , and V_{OHP} waveforms.

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AC Performance

AVC propagation delays are typically near 1 ns when tested in accordance with the standard 30 pF loading at room temperature and 2.5 V V_{CC} . Figures 11 through 16 show simulated device behavior as a result of variations in temperature, capacitive loading, and multiple output switching.

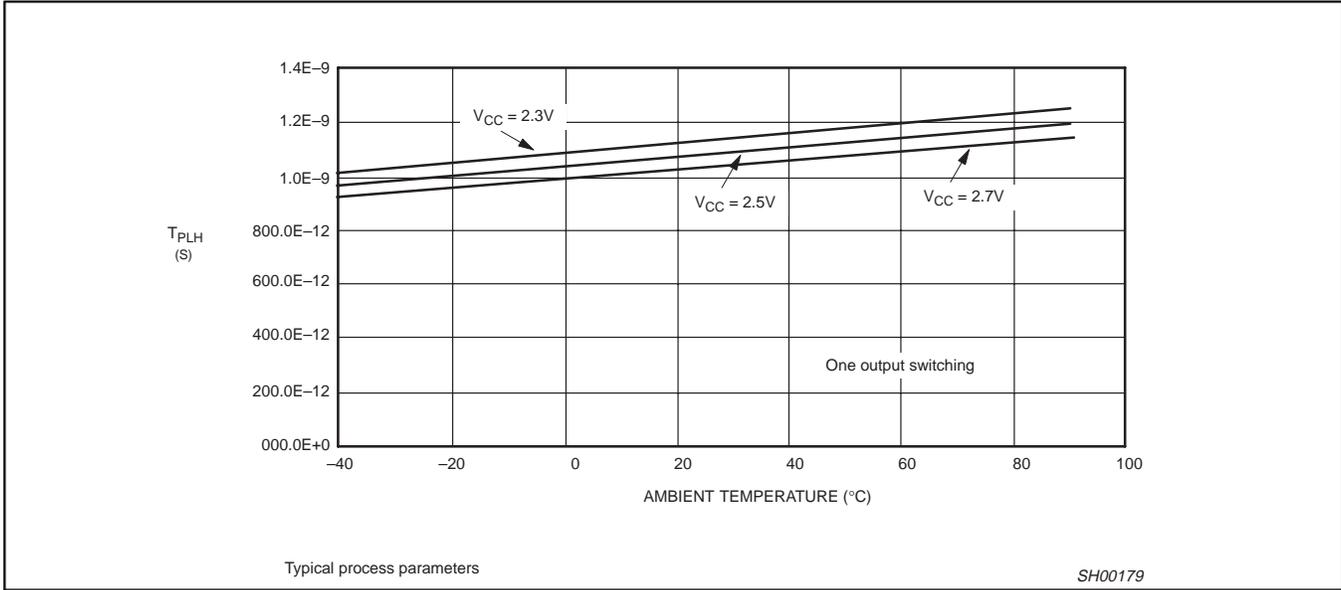


Figure 11. T_{PLH} vs. temperature

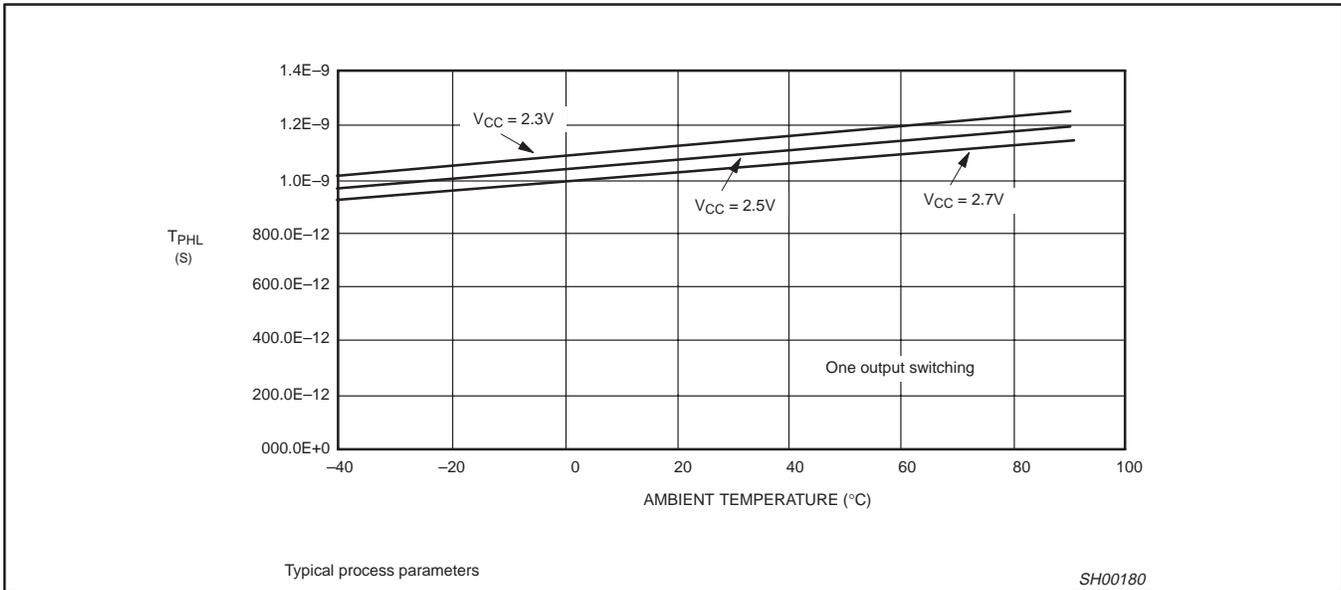


Figure 12. T_{PHL} vs. temperature

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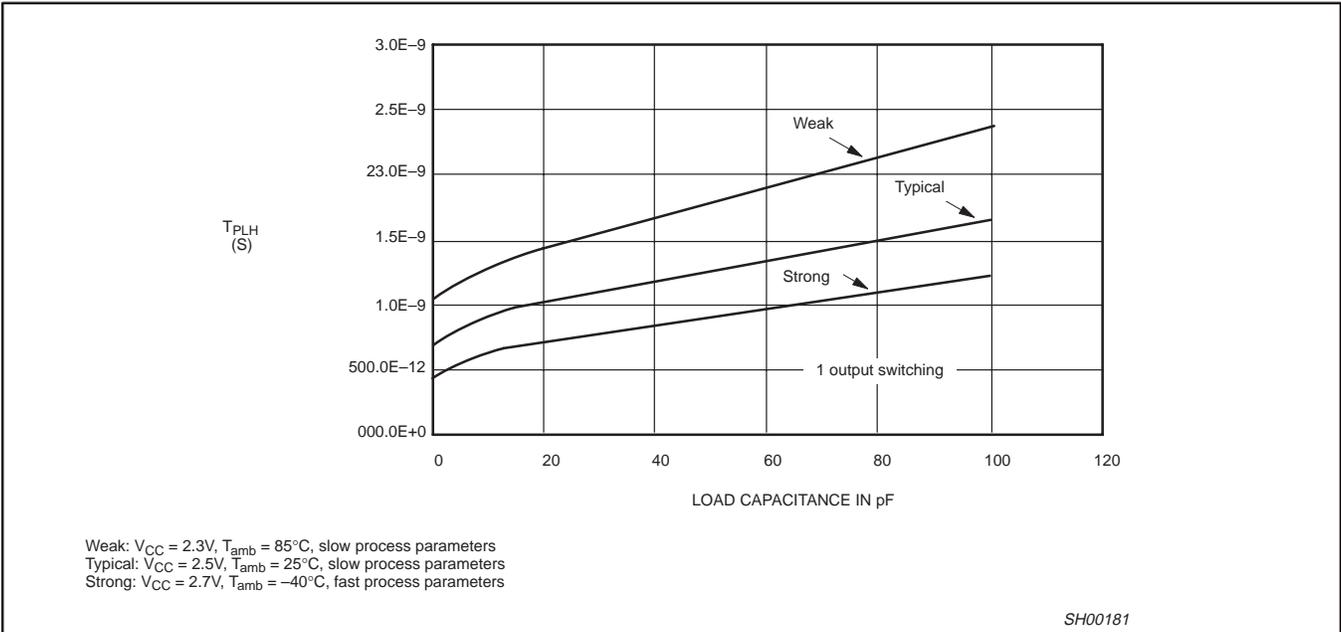


Figure 13. T_{PLH} vs. load capacitance

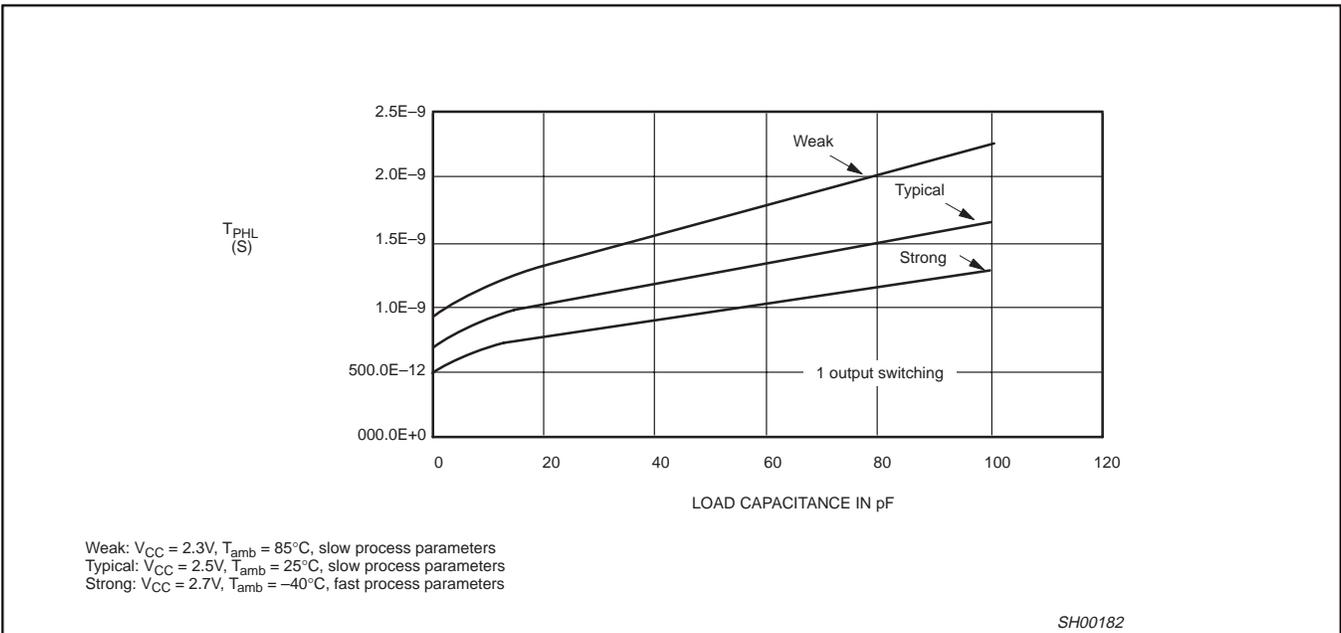


Figure 14. T_{PHL} vs. load capacitance

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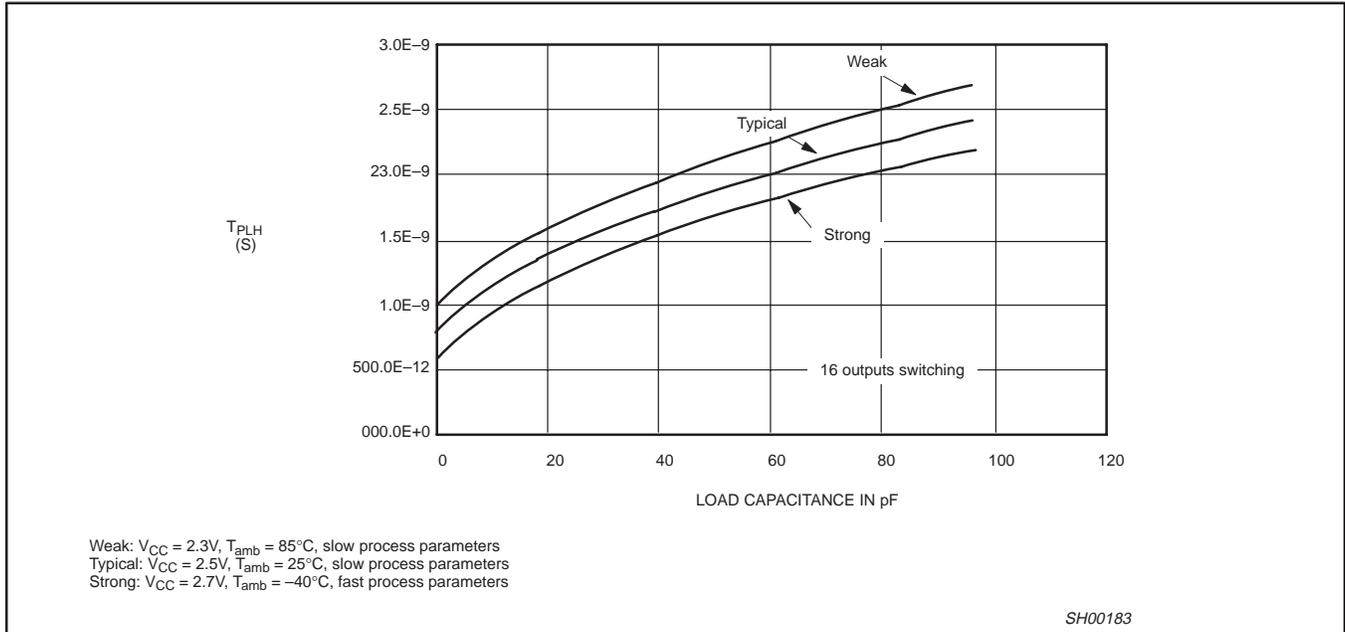


Figure 15. T_{PLH} vs. load capacitance

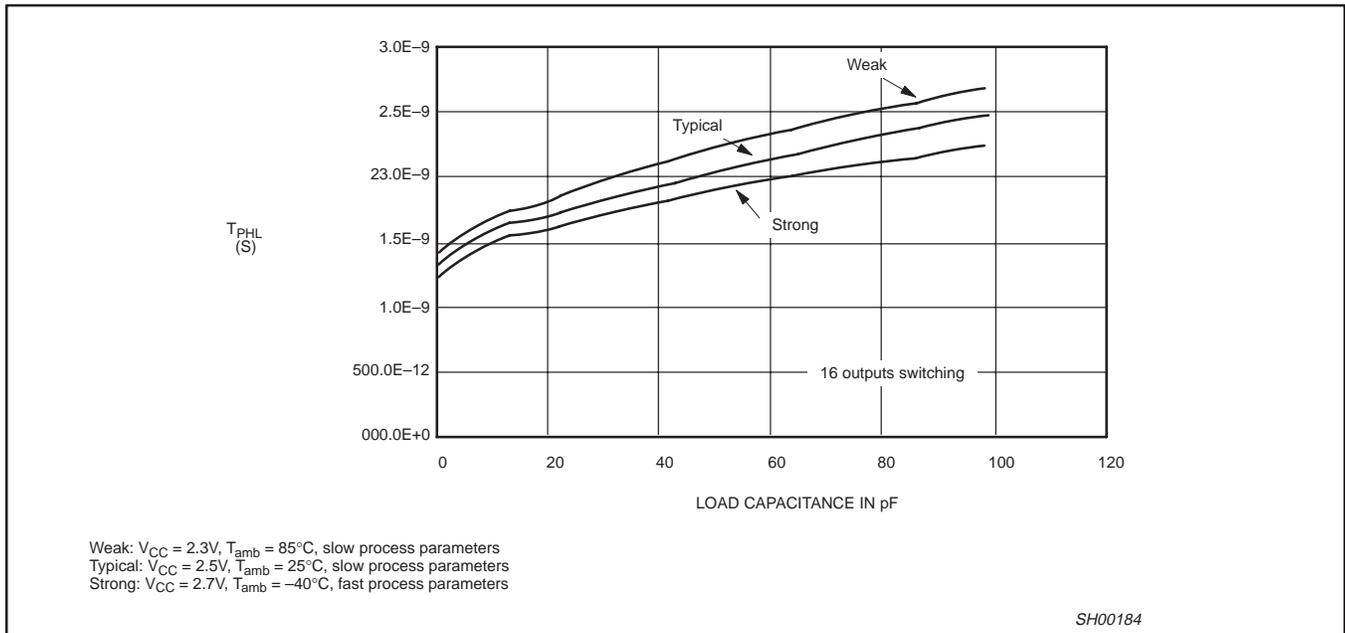


Figure 16. T_{PHL} vs. load capacitance

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PC133 SDRAM REGISTERS

Two to three AVC16834/835/334/836s constitute the memory logic interface for Single Data Rate (SDR) PC133 SDRAM memory modules as specified by the JEDEC 42.5 standard. With the help of faster registered drivers, PC133 offers a 33% performance boost over PC100. The AVC16835/334 are 18-bit/16-bit registered drivers that provide address and control signals to SDR PC133 SDRAMs. The AVC16834/836 are 18-bit/20-bit registered drivers with inverted register enables. The AVC16834/835/334/836 provide the logic solution for SDR PC133 enabled applications.

Conclusion

The AVC family offers a solution for new designs needing the highest performance in 1.8 V, 2.5 V, and 3.3 V systems. Its DCO™ circuit enables blazing sub-2 ns speeds while maintaining very low switching noise. AVC offers a line of bus interface functions for today's high performance, low voltage systems.

Acknowledgements

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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