

APPLICATION NOTE

AN203

Test fixtures for high speed logic

1998 Apr 02

Test fixtures for high speed logic

AN203

INTRODUCTION

The Philips Semiconductors Logic Product Group (LPG) operates a Characterization Laboratory in Albuquerque, New Mexico. This Lab maintains the capability of testing the 11 logic product families the Group supports. These include: BiCMOS ABT, ABTH, LVT, ALVT, FAST-74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL.

Due to the great diversity of product families and the different testing requirements and complexity of the product types of each family, Philips Semiconductors LPG Characterization has designed and built a bench test AC fixture that is specifically designed to address to only the High-speed logic families. It has the advantages of being very versatile, has high bandwidth capability ($\geq 750\text{MHz}$), is 50Ω system compatible, and is manually programmable for the input static voltages. This provides the ability to have one fixture that addresses many product types across families. The extent of this versatility is explained in the following Application Note. The families that this fixture is intended to support are: FAST, ALS, ABT, LVT, ALVT (Note: This fixture is compatible with any 500Ω pull-down load.).

THEORY OF OPERATION

There are several key points in testing the faster edge-rate logic families. They are:

- Very good bypassing and decoupling (they are different).
- Large ground and V_{CC} planes
- Low-impedance signal lines (i.e., 50Ω)
- Signal lines that are uniform in impedance over frequency
- Signal lines must have high bandwidth ($>500\text{MHz}$)
- Low-inductance paths for the DUT leads, including V_{CC} and GND
- Output AC load close to the DUT
- Measurement point close to the DUT
- Avoidance of ground loops (especially on inputs at DC levels)

Also of concern to the test engineer and the manager are:

- Versatility and/or ease of use (there are tradeoffs)
- Cost
- The number of fixtures needed to support products

Each of these concerns have merit and must be understood by the user of these logic families if valid and correlatable results are to be found.

V_{CC} and GND

The secret in V_{CC} and GND use in fixturing is to do the things that reduce the noise that can: 1) get to your part, and 2) come from your part. This is done by reducing the noise of the V_{CC} as it arrives to the fixture, by judicious application of frequency dependant bypassing at the DUT V_{CC} pin to GND and reducing inductance from the V_{CC} and GND pins of the DUT to the point where good contact of the bypassing and V_{CC} and GND planes occur. All of these are techniques used in good RF and microwave board design. By reducing parasitic inductances and cleaning up any sources of noise, good signal integrity is better maintained.

These points are evident in the fixture Philips Semiconductors has designed. Part of the noise reduction of the power supply as it arrives is done by bypassing the power supply at its terminals. The power is then brought to the fixture via banana cables, (as short as possible), to jacks on the chassis of the fixture. An 18 gauge wire, attached to the jack, is wrapped through an inch ferric core 8-12 times for decoupling of any spikes. (Details of the cores used are included in the parts list.) This acts as a Low-pass filter. The wire is then soldered to the bottom of the PC board onto the large V_{CC} plane that narrows to the V_{CC} bus running between the pins of the DUT. See Figures 1, 2, and 3 for detail.

Triangle-shaped, the V_{CC} plane provides a Low inductive path for the V_{CC} to the DUT pin. See Figures 2 and 3 for the board layouts. The V_{CC} bus from this plane travels down between the DUT pins to that connection. This is so connection to the V_{CC} bus is easy and very short. The DUT may have V_{CC} located on any pin with this configuration. The pin is connected to the V_{CC} bus by soldering small copper braid or similar Low-inductance wire capable of carrying the current for the device, see Figure 4.

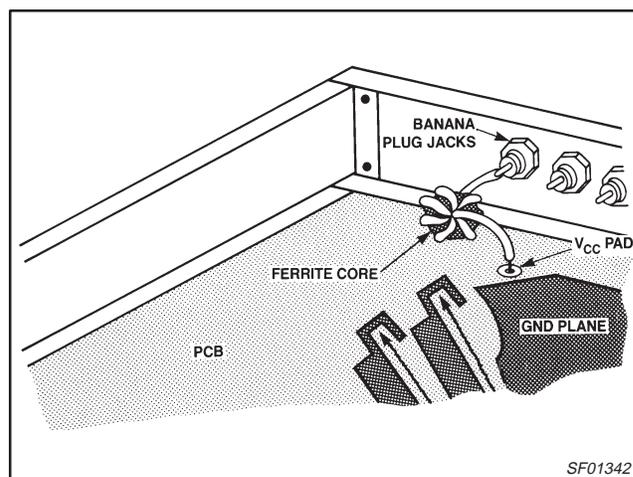


Figure 1. Underside View of PCB Fixture Ferrite Core Placement

Test fixtures for high speed logic

AN203

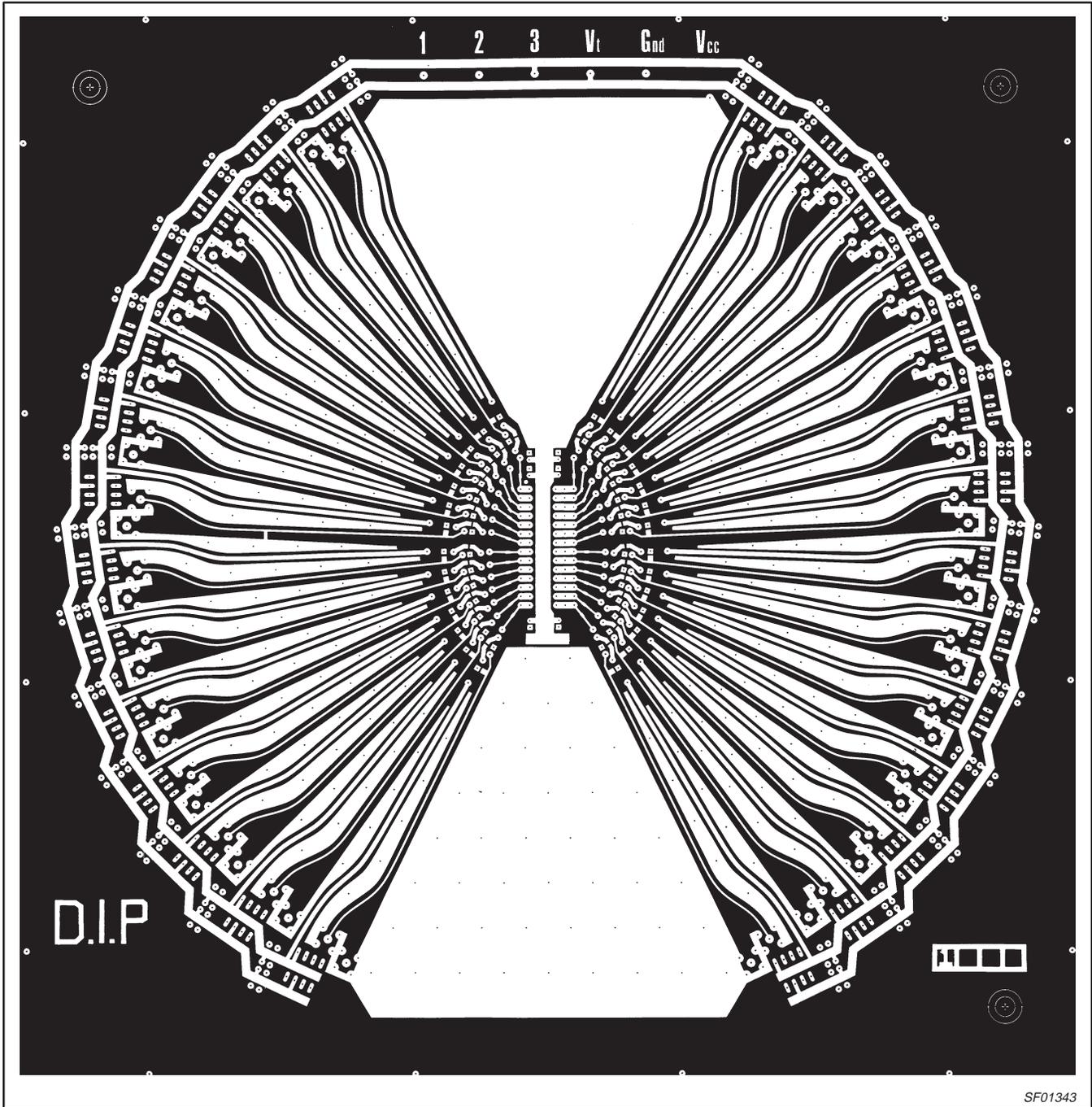


Figure 2. Board Layout — Top Side

Test fixtures for high speed logic

AN203

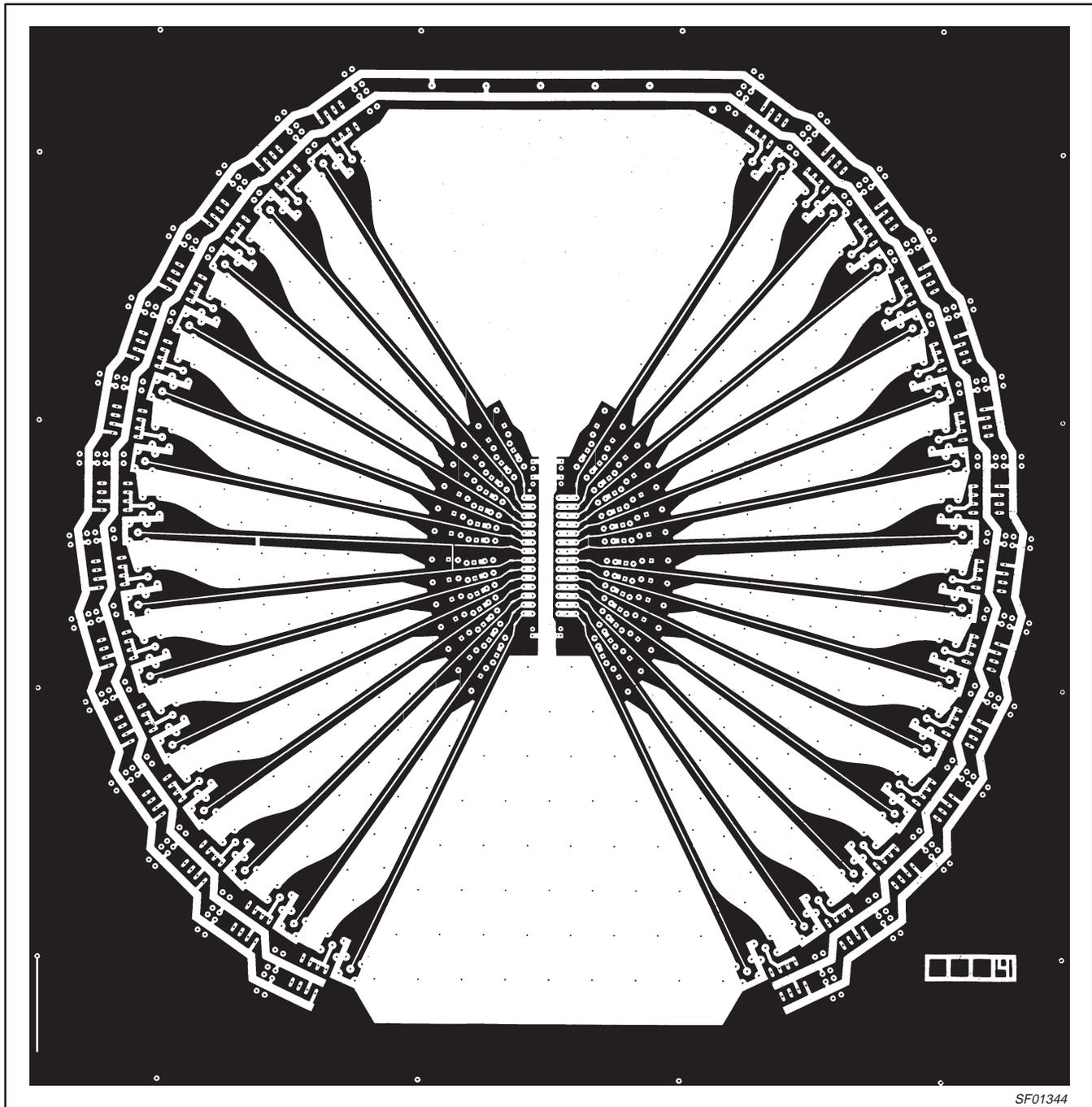


Figure 3. Board Layout — Bottom Side

On the opposite side of the top layer of the board is a triangle-shaped ground plane. Ground planes are also located on the bottom layer of the board in the same places as the V_{CC} and ground planes of the top layer. Since this fixture is laid out for 50Ω stripline, layers 2 and 3 are almost total ground plane, with holes in them for feed-throughs and components. Also found between the signal lines, on the top and bottom layers, are ground plane “fingers” that are connected to all 4 layers by plated-through holes. This provides good separation of the signal lines resulting in lower cross-talk.

The bottom layer ground plane consists of two triangle-shaped planes connected by a bus strip that runs between the DUT pins. This was done for 3 reasons: First, this allows connection of any ground pin of the DUT to the ground, regardless of location; like the V_{CC} connection on the top layer. Second, it allows the connection of the bypass capacitors from the V_{CC} pin to the ground with the shortest possible lead length. Characterization uses typically 2 or 3 ceramic chip capacitors and 1 or 2 dipped tantalum capacitors (35V) to bypass the V_{CC} pin. It is important to keep the dipped tantalum capacitor’s leads as short as possible to reduce series inductance.

Test fixtures for high speed logic

AN203

The recommended values of capacitors are: 100pF, 0.01μF, 0.1μF and 10μF. We have found at times, the need to adjust these values depending upon the product type and its performance. Some noise sensitive circuits need more bypassing in the lower and extreme higher values of capacitance. And third, the connection of the two planes eliminates possible ground loops and the feed-throughs create a ground mesh and give an excellent ground plane for the circuit. Figure 4 illustrates the bypass connections.

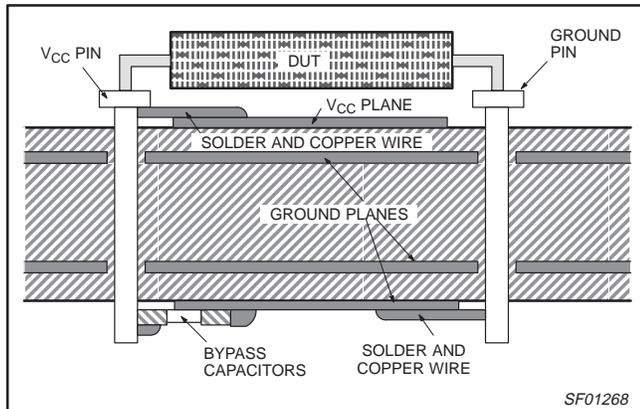


Figure 4. Decoupling Connections

BYPASS AND DECOUPLING

It is important to understand the difference between decoupling, as with the ferrite core, and bypassing, as with capacitors. Decoupling occurs as High-frequency signals are removed by saturation of the ferrite core. This prevents "noise" that may be on the V_{CC} power supply from getting on the V_{CC} plane. The action of the bypassing capacitors is to: 1) "pass" any non-DC signals that occur on the V_{CC} (due to the part's operation) to ground, and 2) be able to provide the "instantaneous" current demands of the part as it switches.

The various values of capacitors are intended to provide a Low-impedance path at all operating frequencies. Since real-world capacitors have resonance points at a given frequency, depending upon their value and type of capacitor (and actually turn inductive above the resonance point), using different values that have different resonance points allows an across-frequency Low-impedance path for V_{CC} noise.

An important point in the use of bypass capacitors is the minimization of lead length. Lead length represents inductance; inductance in series with the capacitance. If it is too much, it can cause resonance and oscillation problems with the part and/or power supplies and nullify the benefit of the capacitors. It also plays a major part in inhibiting the effect of the "instantaneous" current response needed by the part from the bypass capacitors. It actually can cause the ground of the device to track the change in current to the degree of the lead inductance. The lower the inductance, the lower the "ground bounce" effect. Hence, short or no lead lengths on capacitors are needed to help prevent the effects of ground bounce.

SIGNAL LINES

A signal line is defined as a line that carries the input stimulus, either DC or AC, or output response, to or from the device. Since these signals are measured and determine the data which characterizes the part, it is critical that they are of the highest integrity and represent, as far as physically possible, the action of the part; not the nuances of the fixture. To achieve this, the line must not be able to change the signal over the measurable frequencies of the device, nor affect the delay of the part.

The fixture as designed, has 50Ω signal lines determined by a stripline layout method. The 50Ω value was selected for several reasons:

1. The 50Ω value matches impedance with the pulse generators that are used as input stimulus.
2. The output loads specified for this fixture are either a 500Ω pull-down or a 50Ω pull-down (ECL), in parallel with a capacitive load. This allows the 50Ω signal line to be terminated into this load for either a 10:1 or a 1:1 match.
3. A Low-impedance line will have better characteristics with regards to cross-talk and resisting external noise.

There are two types of signal lines on this fixture: input and output; both of which are 50Ω transmission lines. The input line is on the top side of the board and is always terminated in 50Ω. It is connected to the DUT via a 0.3" jumper, Jumper #1 for input. When this jumper is installed, the DUT pin is available only as an input. To allow this line to be used as an output, a 0.1" jumper, Jumper #1 for output, is used instead of the 0.3" jumper. This connects the DUT pin to the AC load when the DUP pin is an output. See Figure 6.

The output signal line can be dedicated two different ways. The first method, used for ECL, is to leave shorted the 50Ω trace and have it run directly into the SMB connector into the 50Ω sampling system. The second method is to cut the trace at the DUT pin and solder the 450Ω chip resistor, R1, across the cut. This, combined with the 50Ω scope, then appears to the part as either a 500Ω probe for the input signal or the 500Ω output AC load for the output signal.

The signal lines are equal length and therefore do not introduce any extraneous delay from pin to pin. We also characterized the impedance of the lines over frequency to ensure minimal distortion over the frequency range and any effective change in propagation delay caused by the relationship of inductance and group delay, see Application Note AN202. Figure 5 illustrates the frequency response of the signal lines in impedance.

This is considered to be high bandwidth and encompasses the frequency range exhibited by ALS, ACL, ECL, and FAST logic families.

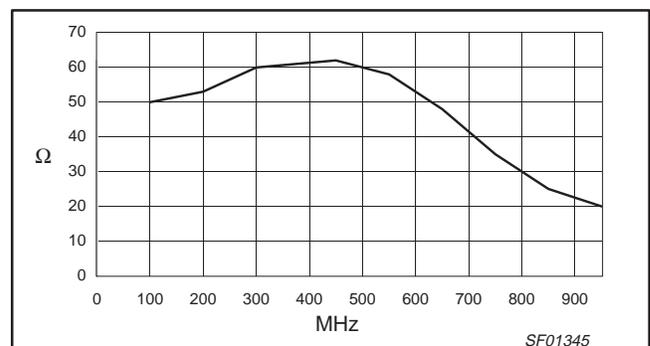


Figure 5. Signal Line Frequency Response

Test fixtures for high speed logic

AN203

LOADING

The explanation of the two types of AC loads that may be used will be covered in two parts. First the ALS, ACL, and FAST implementation will be discussed, then the ECL implementation.

ALS and FAST Implementation

The FAST and ALS product families AC load is specified as a 50pF capacitor and a 500Ω resistor in parallel. This load has the advantage of being adaptable to both a High-impedance (A. T. E.) or a Low-impedance (bench) measurement environment. The Philips Semiconductors fixture uses a Low-impedance environment primarily for two reasons. The first reason is that experience of the last 5 years has told us that High-impedance present a reliability concern and can introduce hard to detect errors into the waveform.

The second reason being that most suppliers of these technologies provide data based upon the Low-impedance approach and most large users of these products do so as well. This also allows the fixture to be used for ECL testing since that product uses a totally 50Ω environment. Figure 6 illustrates how this test fixture implements the 50pF/500Ω load schematically.

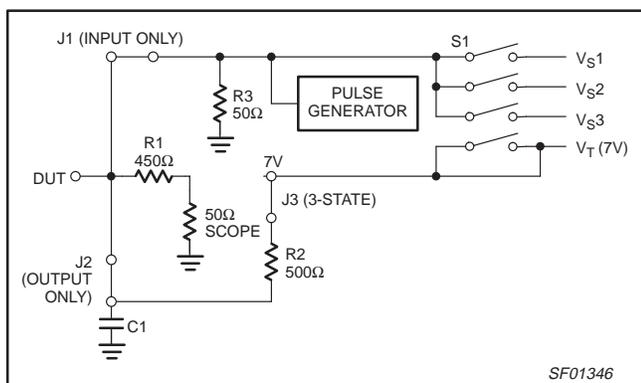


Figure 6. PCB Fixture Schematic

The fixture was laid out to present the load as close as possible to the device, and yet allow for flexibility in deciding if a certain pin is an output or an input. This distance is critical due to its inductive effect upon ground bounce phenomena. It is acknowledged here that a fixture dedicated to a single device type without jumpers, and therefore placing the load virtually on the pin of the device, would show the ground bounce phenomena for simultaneous switching to be less than that of this fixture. However, this fixture can be so

dedicated by not using the pads as provided, but rather by using the ground bus, like the bypass capacitors used. The flexibility of this fixture substantially reduces the cost of fixturing for these families. Studies on simultaneous switching with this fixture have shown dramatically favorable results to previous fixtures. Those studies continue. For work other than that of simultaneous switching, there will be no appreciable difference with a dedicated fixture.

As illustrated in Figure 7, the load is shared with the 50Ω input of the measurement system; a 50Ω sampling oscilloscope. The 450Ω resistor: R1, is soldered to the socket pin of the device and is in series with the 50Ω input of the scope. Figure 7 illustrates this on the board layout of one input/output pin. This allows virtually a probe tip on the device pin. The load capacitor: C1, is a 33pF ceramic chip capacitor. This is added to the measured value of 17pF of board capacitance, achieving the 50pF value specified for the load. The distance from the pin to the capacitor is 0.5 inches and is adequate for the testing of these product families.

For testing 3-State parameters, the 500Ω resistor: R2, is connected to its pull-up supply. V_T via a 0.3" jumper: Jumper #2. The V_T supply is bussed to each pin and may or may not be connected with that jumper. See Figures 6 and 7.

Input Stimulus and Measurement

When the input is not used for a signal input, the line may be switched to one of three voltage sources: V_{S-1} through V_{S-3} , by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor: R1, pulls the line to ground and can be used as a hard low level. See Figure 6. These voltage levels are brought in from external supplies through banana connectors like V_{CC} . This scheme eliminates excessive cabling to each input to provide the static input levels and thereby reduces parasitic inductances and cross-talk. Each of the 3 busses and the V_T bus all have places for bypass capacitors in the event of noise on the static levels. Figure 8 illustrates the DIP switch and SMB connectors and how they control the input stimulus and output measurement.

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is compatible with SMC; it is push-on, it is small for easy configuration, and it is capable of high bandwidth operation. Figure 8 illustrates where the connections are made, where the pulse generators connect to the input and an SMB connector. Since the 450Ω resistor: R1, is soldered directly to the pin of the device, the actual probe tip is at that point. See Figure 7. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

Test fixtures for high speed logic

AN203

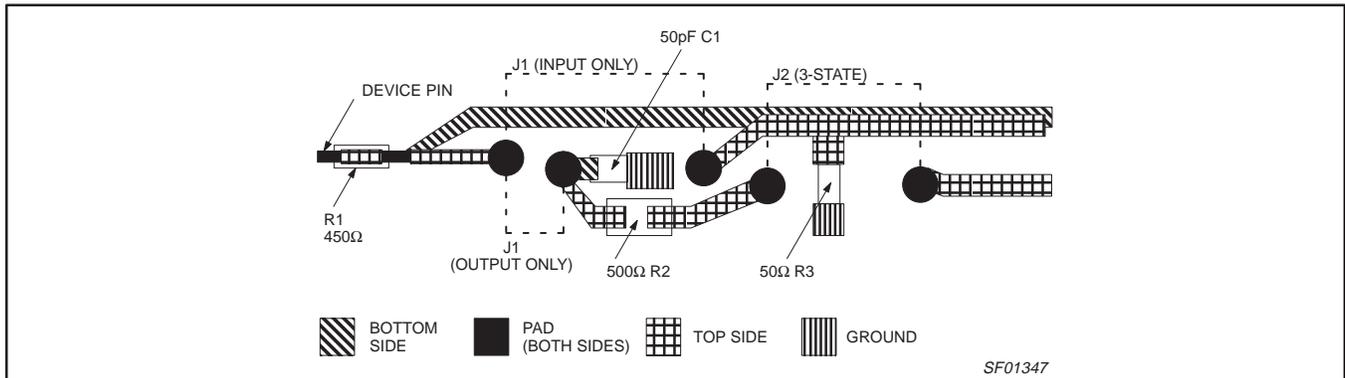


Figure 7. Fixture — Board

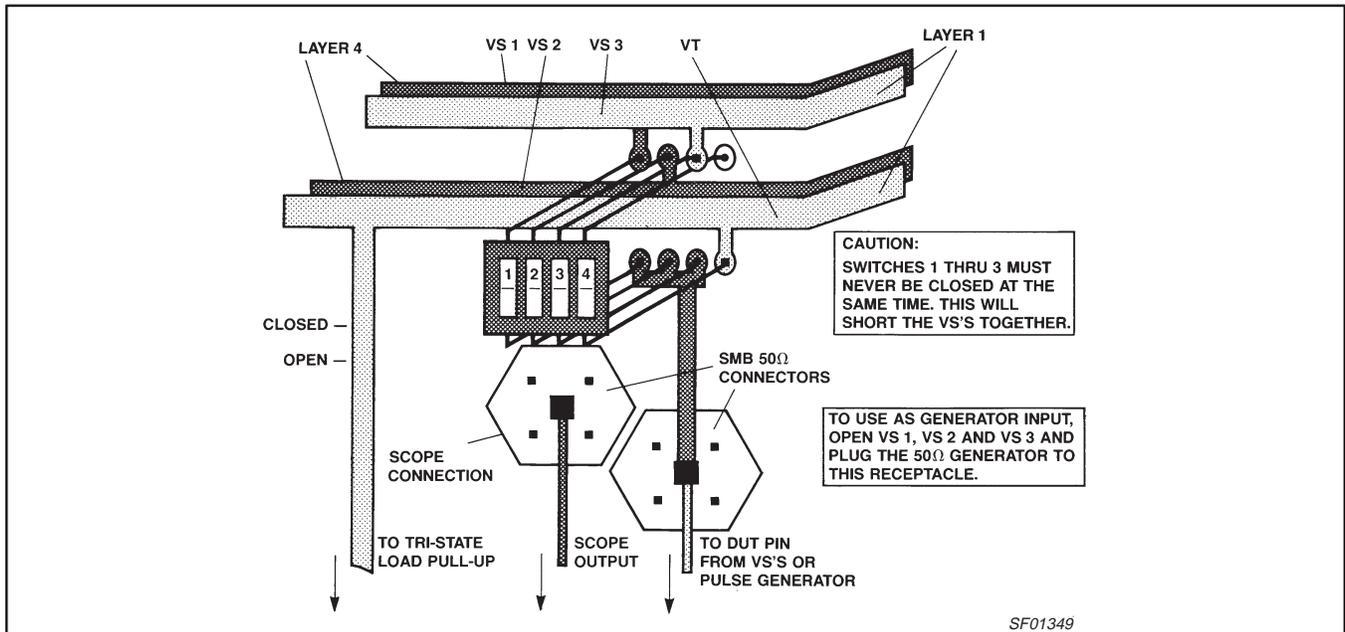


Figure 8. DIP Switch Connection for V_{S-1} , V_{S-2} , V_{S-3} , and V_T and the SMB Connectors for Input Signals and Output Measurement

Test fixtures for high speed logic

AN203

Versatility and Cost

At some point, there is a choice between the most technically attractive options and the cost of options. This fixture has been primarily designed to optimize the cost effectiveness of test fixturing yet yielding a technically sound tool. To do this, a compromise has been made between the ease of use and the versatility.

In the construction of the fixture, a choice is made as to where the V_{CC} and GND pins are to be located. This then dedicates this particular fixture to part types with this V_{CC} and GND configurations. This is also done with a dedicated fixture. However, on a dedicated fixture, the pins are individually constructed to be either an input or an output, and in so doing, the fixture is usable for 1-to-4 devices. The Philips Semiconductors fixture, once dedicated to a particular V_{CC} and GND configuration, is built up to have both input and output components on all signal pins. The selection of which pin is an output or an input is made by inserting the appropriate jumper. See Figures 5 and 6. The same applies in doing 3-State testing. The tradeoff here is that it would probably take less time to setup the dedicated fixture than the Philips Semiconductors fixture. To help compensate for that tradeoff, we have the three V_S supplies that may be switched into any pin to provide input static levels and eliminate the need to bus input High or Low levels by external cabling. For the user that means the only connections being made to the fixture are:

- The V_{CC} (banana jack)
- The (GND) (banana jack): this is the common ground of all input supplies.
- The V_{S-1} , V_{S-2} , and V_{S-3} supplies (banana jack): these may be any voltage and are switchable. Philips Semiconductors connects programmable supplies to these connectors.
- The V_T supply (banana jack): this is the 3-State pull-up voltage and is permanently connected to the bus to each pin. It is selectable by Jumper #2, see Figures 6 and 7. For FAST and ALS products this is 7V. For ACL products this is $V_{CC \times 2}$ and it is not used for ECL applications.
- Input Stimulus (inside SMB connector: this is found on every input/output pin. More than one pin may be used in this manner.

CAUTION: When using this connector as an input stimulus, make sure V_{S-1} – V_{S-3} are disconnected. This will short the power supplies to the generator if they are not disconnected.
- Output Measurement or Scope Connection (outside SMB connector: this is also found on every input/output pin. More than one pin may be used in this manner. Remember, if this pin is not connected to a scope and is an output, a 50Ω resistor must be connected here to ground to complete the 50Ω resistive load. Philips Semiconductors has constructed 50Ω load by soldering a high-quality (High-frequency) 50Ω resistor inside a female SMB cable connector. See Figure 9.

CAUTION: V_S 1,2 and 3 are all on the same DIP switch. Since they connect to the same bus per pin, **ONLY ONE SUPPLY MAY BE CONNECTED AT ONE TIME**, Otherwise, this will result in a short between power supplies connected.

With these 6 connections, the fixture is capable of testing the product lines as mentioned.

The cost of this fixture ranges from 550 per fixture, dedicated to a 20-pin device in quantities of 1-10, to as low as 385 per fixture of the same type in quantities over 100. This is not substantially higher than the cost of a dedicated fixture; which is estimated at 200- 500. The factor to consider would be the quantity of fixtures for the number of products to be tested. To have a dedicated fixture for every 2-3 product types versus a “universal” test fixture for 20-30 product types is worth considering from a cost standpoint.

Included in Appendix 1 is the parts list for this fixture and the supplies used by Philips Semiconductors. This in no way constitutes Philips Semiconductors endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offered to the public to duplicate and use within their own environments. Philips Semiconductors will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Philips Semiconductors has no control over those issues. The intent is to provide something for users of High-speed logic that has been proven and tested in a true High-speed use, and provide a characterization of these products prior to their introduction to the market place.

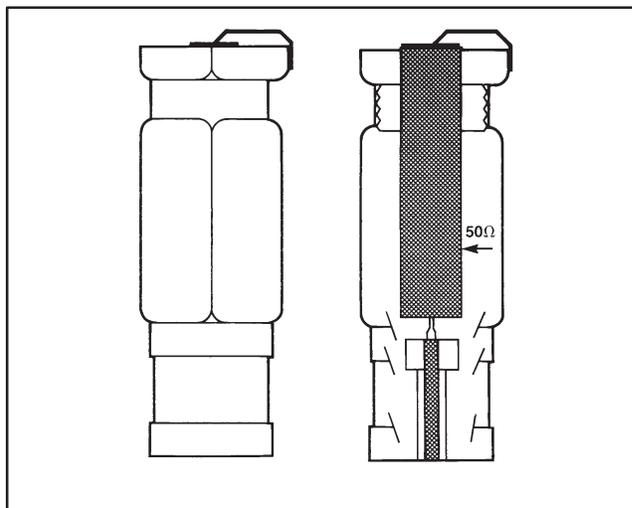


Figure 9. 50Ω Load Resistors Using Output Pin SMB Cable Connectors

Test fixtures for high speed logic

AN203

APPENDIX 1 — COMPONENT AND VENDOR LIST

The following prices are quoted for a 30 piece build of a 24 pin test fixture and are not binding in any way.

COMPONENT AND VENDOR LIST

ITEM		PART TYPE		REQUIREMENT	SUPPLIER
Printed circuit motherboard	SO and SOL	#SD8512.28		1 part per configuration	
	DIP	#SD8512.31			
SO and SOL sockets (SOIC through hole socket)		14 pin	001-014	1 part per board	Surface Mount Devices, Inc. PO Box 16818 Stamford, CT 06903 (203) 322-8290
		16 pin	001-016		
		16L pin	001-116		
		20 pin	001-120		
		24 pin	001-124		
		28 pin	001-128		
Socket terminal pins	For DIP boards	LSG-1AG14-1		Number of pins equal to the part pin count times by (7) seven. $24 \times 7 = 160 \times .20 =$	
	For SO and SOL boards			Number of pins equal to the part pin count times by (5) five. $24 \times 5 = 120 \times .20 =$	
Shorting blocks (jumper)		0.3 inch	8136-475G1	1 part per pin cost per part $\times 24 =$	Augat
		0.2 inch	8136-651P2		
Chip resistor		50 Ω 1%	CRCW 1210	1 part per pin cost per part $\times 24 =$	Dale Electronics, Inc. 2300 Riverside Blvd. Norfolk, NE, 68701 (402) 371-0080
		450 Ω 1%	CRCW 1206		
		500 Ω 1%	CRCW 1206		
Chip capacitor (ceramic)		33 pF	500R15N330JP	1 part per pin	Johanson Dielectric
		15 pF	500R15N150JP4	1 part per board cost per part $\times 1 =$	
		0.015 μ F	500S41W103P4		
		0.1 μ F	500S41W104P4		
Dip Tantalum capacitor		10 μ F	106k025NLF	1 part per board cost per part $\times 1 =$	Mallory
		47 μ F	476k020WLG		
Ferrite core			T80-1	1 part per board cost per part $\times 1 =$	Amidon Associates 12033 Otsego Street North Hollywood, CA 91607 (818) 760-4429
Mounting screw		4-40 \times 1/4 Philips pan head machine screw		16 parts per board cost per part $\times 16 =$	Bonneville Industry Supply Co. 40 So. 1500 W., Orem, UT (801) 225-7770
Banana plug jack		H.H. Smith type, White	1509-101 (order code: 28F1178)	6/board-color your choice cost per part $\times 6 =$	Newark Electronics
		H.H. Smith type, Red	1509-102 (order code: 35F870)		
		H.H. Smith type, black	1509-103 (order code: 35F869)		
		H.H. Smith type, green	1509-104 (order code: 28F1179)		
		H.H. Smith type, blue	1509-105 (order code: 28F1180)		
		H.H. Smith type, yellow	1509-107 (order code: 28F1182)		

Test fixtures for high speed logic

AN203

COMPONENT AND VENDOR LIST (continued)

ITEM	PART TYPE		REQUIREMENT	SUPPLIER
Switch	4-bit side actuated piano-dip	76PSB04	1 part per pin cost per part $\times 1 =$	Grayhill Co.
Connectors	Snap on SMD	51-051-0000-220, straight jack receptacle	2 parts per pin cost per part $\times 48 =$	Sealectro
Mounting frame	Philips Semiconductors number CB-10		1 per test fixture	Electronic Chassis Corp. 468 North 1200 West Lindon, Utah 84062 (801) 785-9113
Hookup wire	No. 18/20 gauge Teflon coated		24 inches per test fixture	

The following components may be needed in use of the test fixtures but are not part of the test fixtures

61-001-0000-89	50 Ω terminator plug
51-007-0000	Straight Cable Clamp Type
51-083-0000-222	"T" adaptor J-J-J
51-085-0000	"T" adaptor J-P-J
51-072-0000	Adaptor J-J
51-073-0000	Adaptor P-P
51-001-0020	Shorting plug
61-002-0000-89	50 Ω terminator jack

Supplier:

APPENDIX II — CONSTRUCTION HINTS

A suggested order of assembly is as follows:

1. Cut traces for 450 ohm resistor. (Not needed for ECL).
2. Install SMB connectors. Note: Elevate base from board 0.05".
3. Install DIP switches. Note: Numbers on switches may not correlate to Vs supply numbers.
4. Install Augat socket pin.
5. Install load/termination resistors and capacitors.
6. Strap V_{CC} and GND pins to appropriate bus strips.
7. Install bypass capacitors.
8. Clean flux off of board and components.
9. Check for lead to frame shorts on PLCC board. (Not discussed in App note).
10. Install banana jacks on frame.
11. Attach board to frame with 1/4 Philips pan head machine screws.
12. Wrap wire 8-12 times around ferrite core. Leave enough wire to connect to frame and board. See Figure 1.
13. Connect V_{CC}, GND, and voltage supplies from banana jacks to board.
14. Remove all remaining flux. Keep "flus-off" from banana jacks.

Hints on construction:

- A 0.05" shim that fits under the SMB connector base helps elevate it during construction.
- Mount the SMB connector with flat side out rather than point side out. See Figure 8.
- Solder Augat socket pins in with a part inserted to hold the pins steady.
- "Piano DIP" switches have the numbers reversed from the board notation. Taping a new number on the board designations will help match the switches.
- Hints for solder chip components: apply a small amount of solder on one side of the pads on the board.
- Keep DIP switches and SMB connectors spaced as far away from each other as the holes permit, i.e., push the SMBs in and the DIP switches out.

Test fixtures for high speed logic

AN203

NOTES

Test fixtures for high speed logic

AN203

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998
All rights reserved. Printed in U.S.A.

Date of release: 04-98

Document order number:

9397 750 05218

Let's make things better.