AN1548

Guidelines for Debugging the MC44011 Video Decoder

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INTRODUCTION

Normally, the implementation of the MC44011 Multistandard video decoder is fairly simple in that there are no external adjustments, or critical components, to deal with. However, since this IC contains several interrelated functions and a substantial amount of programmability, debugging an improperly working circuit can sometimes be daunting. The purpose of this document is to provide a procedure for debugging and checking the operation of this IC, and an indication of what to expect at some of the various pins.

PRELIMINARY

First some basic facts about this circuit (to hopefully clear up some common misconceptions):

- The recommended components shown in Figure 1 are valid for both NTSC and PAL signals. None of the external components need to be precision tolerance or adjustable. The crystals need to meet the specifications in Table 1.
- If the horizontal PLL is not locked to the incoming video, *nothing else will work correctly.* The first step in debugging is to get this PLL properly locked up.
- The pixel clock (at Pin 18) is not related to either of the crystals, and the crystals' functions are not related to the pixel clock. These circuits function independently of each other.

There were some mistakes in the original printing of the MC44011 data sheet which need correcting:

- In Figure 42 of the data sheet, the capacitor at Pin 12 should be 470 pF, not 4700 pF.
- In Figure 42 of the data sheet, Pin 27 is the Green input, and Pin 28 is the Red input.

HELPFUL HINTS

- Have a copy of Appendix A with you at all times when working with the MC44011, as it is a summary of all the software control bits, DACs, and flag information.
- Use a dual trace scope when looking at various waveforms at the IC pins. Lock channel one to the incoming video, and use channel two to monitor other waveforms. A horizontal sweep of 10 μs/div is good in most cases.
- A scope with a Video Triggering feature, where the scope can lock to a particular line in the field, can be extremely useful. This kind of triggering eliminates the artifacts on the scope associated with the vertical interval, and can allow you to check performance line–by–line if necessary.
- Ensure that the video signal used to check the IC's performance is a good quality signal conforming to NTSC or PAL standards. Generally, signals from a VCR are not the best of quality as they contain jitter and noise. A video generator should be used so that the video source is not in question.
- The MC44011 should be checked in the sequence listed below, as the operation of some sections depend on the proper operation of other sections.

SUPPLIES, GROUND

The 5.0 V supply applied to Pins 19, 23, and 40 must be clean and free of ripple. The PLLs within the MC44011 are sensitive to ripple, and consequently will produce additional jitter if the supply is not clean. There should be a 10 μF bypass capacitor adjacent to each of these pins.

There are four ground Pins (10, 17, 24, 39), and they must all be connected, preferably to a ground plane. It is important that the components at Pins 9 and 11 be connected close to the pins, and to the ground at Pin 10.

The MC44011 requires ≈135 mA (including the current at the RGB outputs). The MC44140 delay line requires ≈35 mA.

SOFTWARE CONTROL

Basically, the MC44011 cannot be used unless proper communication on the I^2C bus is established, since there is no guaranteed power–up condition for the various registers within the MC44011. The only exception to this is control bit \$86–6 which always powers up as a 1, disabling the horizontal PLL. The initialization routine must set this to a 0, followed by writing \$00 to register \$00, to allow this PLL to operate.

If a problem is suspected with the I^2C bus, it is best to check it with a scope rather than only a signal analyzer. With the scope, make sure the setup and hold times are correct, and that the acknowledge bits are occurring as expected. None of the timing requirements are critical or difficult to meet. Appendix C of the MC44011 data sheet provides a short description of the I^2C bus operation, and its requirements. More detailed information about the I^2C bus can be obtained from Philips Semiconductor.

Ensure that each write operation starts with the address byte \$8A, followed by a sub–register address byte, followed by a data byte – a total of 27 clock cycles. The MC44011 cannot accept writing to multiple registers in a single write operation.

It is *strongly* recommended that the software include reading of the flags, as this is one of the easiest ways to monitor the condition of the various parts of the IC. To read flags, write the address $8B, and then read out the two bytes containing the 16 flags (a total of 27 clock cycles). There are times when a flag indication is more truthful, or meaningful, than observing a waveform on a scope.

HORIZONTAL PLL LOCK–UP

As mentioned above, this PLL must be locked to the incoming video before other parts of the MC44011 can be expected to function properly. This PLL normally requires about 100 ms to lock up and stabilize after the application of a new video signal. The PLL locks to the composite sync information received from the internal sync separator, which can receive its information in one of four ways:

1. In the traditional manner – as part of the composite video signal applied to either Pin 1 or 3.
2. As part of a luma signal applied to Pin 29 (Y2 Input).
3. As part of an RGB signal applied to Pins 26 to 28 (RGB inputs). The sync can be on any one of these pins, or on all three.
4. As composite sync only, applied to Pin 1 or 3, or to Pin 29 (Y2), or to Pin 27 (green input). If sync is applied to Pin 27 only, then Pins 26 and 28 must be ac coupled to ground.

If composite sync only is applied to any of the above pins, it is recommended that it not be TTL levels. If the sync information is TTL, a simple resistor divider can be used to reduce it to a 1.0 to 2.0 V amplitude, and then ac couple it to the input pin.

To check if this PLL is locked, check flag 12 – it should be a 0 (assuming the PLL has been enabled and flag 11 is a 1). This can also be checked with a dual trace scope. With one channel locked to the incoming video (or sync), check the burst gate (Pin 8) on the other channel. If locked, the waveform should resemble those shown in Figure 2, with the timing indicated in Figures 25 and 27 of the MC44011 data sheet. Alternately, Pin 14 (FHref) could be monitored instead of the burst gate.

If the PLL is not locked, check the following:

1. Is PLL1 enabled (is flag 11 = 1)? If not, enable it by setting bit $86–6 to 0, then sending $00 to register $00.
2. If the video is applied to Pin 1 or 3, is the correct input selected with bit $88–7? Check this with the scope by looking at Pin 33 (Y1 Out). The luma portion of the input signal will be visible at this pin. If the wrong crystal is selected, or the color decoder is set incorrectly, the waveform at Y1 will still resemble the luma portion of the signal, as long as Pin 1 or 3 is properly selected.
3. Is the correct Sync Source selected? Check this by setting bit $85–6 to a 1, and then look at Pin 13 on the scope. The composite sync portion of the input signal should be visible on that pin, at TTL levels. If not, check Table 12 in the MC44011 data sheet, and set bits $86–7, $87–7, and $88–6 appropriately.
4. If the above software controls seem to be correct, then the hardware must be checked. Check Pin 11 (PLL1 filter) with the scope's channel 2 set to 500 mV/div, ac coupled. The waveform should resemble that in Figure 3 – flat, except for a 200 to 300 mV blip at each sync time. The dc voltage at Pin 11 should be between 1.5 and 4.0 V (typically around 2.0 to 2.5 V). If the waveform at Pin 11 does not resemble this, check the components at Pin 11. Ensure their values are correct, and that they are connected to Pin 10, which should be connected to the system ground.

VERTICAL DECODER LOCK–UP

Assuming the horizontal PLL is correctly locked up (Flag 12 = 0), then check flag 15. If the vertical decoder is correctly locked, **and** if control bits $77–1 and $77–0 are set to 1,1 (Auto Count), this flag will be a 1.

It is possible, under certain conditions, for flag 15 to indicate a locked condition, and yet the output sync pulses are not properly positioned with respect to the incoming video. The vertical sync output at Pin 4 can be checked on the scope by setting the sweep rate to 2.0 ms/div. The timing of the vertical sync pulse is shown in Figures 33 and 34 of the MC44011 data sheet. The following guidelines apply:

1. If bits $77–1,0 are set to the injection lock mode (0,1), the vertical decoder will correctly lock, but flag 15 will always indicate a 0.
2. If the incoming video is NTSC, and if bits $77–1,0 are set to Force 525 (1,0), the vertical sync pulses will be locked to the video when viewed on a scope, but not at the correct position in the field (see Figure 4 for an example). Flag 15 will indicate a steady 1. If the incoming video is PAL with the bits set to 1,0, the sync pulses will not be locked, yet flag 15 will indicate a 1.
3. If the incoming video is PAL, and if the bits are set to Force 625 (0,0), the vertical sync pulses will be locked to the video when viewed on a scope, but not at the correct position in the field (see Figure 4 for an example). Flag 15 will indicate a steady 1. If the incoming video is NTSC with the bits set to 0,0, the sync pulses will not be locked, yet flag 15 will indicate a 1.
4. If bits $77–1,0 are set to 1,1 (Auto Count), then flag 15 should indicate a 1 if the incoming video is a true interlaced signal, and correctly locked. **CAUTION:** While your laboratory grade video pattern generator may provide a true interlaced signal when set to output a color pattern, there are some generators which change to a non–interlaced (or incorrect interlaced) signal when set to a black–and–white signal, such as a crosshatch pattern. If this type of signal is applied to the MC44011, flag 15 will indicate a 0 even though the output vertical sync pulses are correctly locked. Additionally, the Field ID output (Pin 7) will be a steady high or low, and will not alternate.

In Summary

– When initially attempting to acquire lock (both horizontal and vertical sections are not yet locked (flag 12 = 1, and flag 15 = 0)), set bits $77–1,0 to Injection Lock (0,1) until flag 12 indicates the horizontal PLL is locked. Then set bits $77–1,0 to Auto Count (1,1) for normal operation. Flag 15 should then indicate a 1 after 8 fields of continual lock–up.

– There are very few applications where the Force 525 or Force 625 settings would be useful. It is best to avoid these unless your application can beneficially use them.

Three other items in the vertical section:

1. In addition to flags 12 and 15, check flag 14 (<576 lines) as an additional check that the vertical decoder is properly locked up. This flag will be 1 for NTSC signals, and 0 for PAL signals.
2. The polarity of the Field ID output (Pin 7) depends on the setting of bit $78–7, which affects the timing to the leading edge of the vertical sync pulse. In most applications this timing is not a critical item, so if you have a preference for the polarity of the Field ID, this bit can be used to set that.
3. If you see an extra vertical sync pulse 50 to 60% of the way through the field, then bit $77–5 is set to a 1. Set this bit to 0 to remove the extra sync pulse.

COLOR DECODER

If the horizontal and vertical sections are working properly, the color decoder can now be checked. Discussion of the decoder is relevant only for composite video or S–VHS signals applied to Pin 1 and/or 3. This section does not cover RGB signals applied to Pins 26 to 28, or color difference signals applied to Pins 29 to 31. See the Color Difference Matrix section for those pins.

If black–and–white signals only are being processed, with or without a color burst present, the decoder should be set to the Color Kill mode (see Table 4 in the MC44011 data sheet, or Appendix A), making most of the color decoder irrelevant. The selected crystal, in this mode, will affect only the internal luma delay line. If the application will always involve black–and–white signals only, it is best to inject these into the MC44011 at the Y2 input (Pin 29), bypassing the color decoder altogether.

A large percentage of the color decoder problems experienced by various users were caused by the use of an incorrect crystal. For the decoder to function properly with color signals, the crystal must be the correct type so that it can lock up to the incoming burst signal. The crystal **must** conform to the specifications in Table 1 of this document. The crystal must be a series resonant type for this application, and must be of a type which can be pulled by a PLL. Crystal manufacturers should be consulted before purchasing crystals for this application. Some suggested vendors are listed at the end of this document.

The easiest way to know if the crystal is locked up correctly to the incoming color burst is by observing flag 23 (ACC Active). If it is a 1, the crystal is locked, and the ACC circuit is active.

The crystal, and its series capacitor, should be mounted on the PC board physically close to the MC44011. Depending on the parasitics of the board layout, sometimes it helps to tweak the series capacitor a few pF either way. But if the layout is neat and tidy, this is usually not necessary.

If the crystal is believed to be correct, and a color signal is applied to input Pin 1 and/or 3, and flag 23 indicates a 0, then check the following:

1. Check that the correct crystal is selected with bit $7A–7.
2. If the input signal is composite video, bits $77–6,7 must both be set to 0, and bit $88–7 must be set to select either Pin 1 or 3. Check this with the scope by looking at Pin 33 (Y1 Out). The luma portion of the input signal will be visible at this pin.
3. If the input signal is S–VHS (YC), bits $77–6,7 must both be set to 1, and bit $88–7 must be set to direct the luma and chroma signals appropriately. Please see the description for bit $88–7 in Table 14 of the MC44011 data sheet. If set correctly, the luma signal will be visible at Pin 33 (Y1 Out).
4. Check that the decoder is set correctly (NTSC or PAL) with bits $7C–7,6 and $7D–6 (see Table 4 in the MC44011 data sheet, or Appendix A). Ensure SSD (bit $7A–6) is set to 0, and that HI and VI ($79–7,6) are both 1. (Note: If the decoder is set incorrectly, flag 23 may still indicate a 1 if the crystal is locked up to the incoming burst, but then the output colors will be incorrect).
5. Then check flag 23. If all is working correctly, it should be a 1, indicating that the crystal is locked, and the ACC portion of the color decoder is functioning normally. If this bit is still a 0, recheck the above software controls, and then the following:
   a) Check that the components on the crystal PLL filter pin (Pin 44) are the correct values.
   b) Check the waveform on Pin 44 with the scope's channel 2 set to 20 mV/div for NTSC, and 100 mV/div for PAL – ac coupled. Figures 5 and 6 are examples of the waveform at this pin. The dc level is typically around 2.5 V for NTSC, and 3.5 V for PAL. If the waveform on this pin is near 5.0 V or ground, or has a 50 Hz or 60 Hz ripple on it, either the crystal is the wrong type, or its series capacitor needs to be checked.

Once the crystal has acquired lock and flag 23 is a 1, then the color adjustments within the decoder need to be set (if not already) to obtain correct signals at the color difference outputs (Pins 41 and 42). The color adjustments are the 6–bit DACs (bits 0–5) in the following registers, and the suggested values are decimal values out of a range of 0 to 63:

DAC	Function	Suggested Value
$87–5/0	Saturation	15
$88–5/0	Hue	32
$78–5/0	R–Y/B–Y Rel. Gain	32
$79–5/0	Subcarrier phase	32

With these settings, the color difference and luma signals at Pins 33, 41, and 42 should closely resemble those in Figure 45 of the MC44011 data sheet. If not, recheck the color adjustment settings above.

THE MC44140 DELAY LINE

The MC44140 delay line is needed if PAL signals are being processed, and is not needed if only NTSC signals will be processed. The R–Y and B–Y outputs of the MC44011 go to two sets of inputs on the delay line via coupling capacitors. The capacitors **must** be the indicated values (normal tolerance), or the color processing in the delay line will be incorrect. See the MC44140 data sheet, or Figure 44 of the MC44011 data sheet.

The MC44140 receives its control signals from the MC44011. The clock input (Pin 1) is simply derived from the selected crystal via a capacitive divider, and has an amplitude of 40 to 50 mV_{pp} at 14.3 MHz, and 20 to 30 mV_{pp} at 17.7 MHz. The Sandcastle signal is a timing signal for the delay line, and should conform to the timing and levels shown in Figures 25 and 27 in the MC44011 data sheet. The System Select signal is a dc signal produced by the color decoder in the MC44011, and it tells the delay line that the signals are NTSC (≈1.75 V), or PAL (0 V), or if the color kill mode is selected, or if the auxiliary inputs on the delay line are to be used.

The dc voltage at the various pins of the MC44140 are as follows:

– At the four inputs, and the two outputs: 1.2 to 1.4 V.
– At Pins 1 and 16: 1.6 V.
– At Pins 2 and 13: 4.8 V.

If the video signals are NTSC, the delay line passes them through without modification. If they are PAL, the inputs will have the line–by–line alternating characteristic of PAL (assuming a repetitive pattern is put in), but the output waveforms, to the MC44011, will be steady line–to–line.

COLOR DIFFERENCE MATRIX

This section accepts the R–Y and B–Y signals at Pins 31 and 30 respectively, or RGB signals at Pins 26 to 28. If the color difference signals are from the color decoder section (from Pins 41 and 42), the luma signal (Y1) is supplied internally. Alternately, an external luma signal can be applied at Pin 29 (Y2). Bits $81–7 and $81–6 select which of these two luma signals is active. Note that both signals can be selected to be active simultaneously, while most applications will require that only one be active.

The RGB inputs were designed for standard video level signals (1.0 V_{pp}, nominal), and not TTL level RGB. Sync may be present on any one of the three inputs, or all three.

To obtain the desired output at Pins 20 to 22, various bits must be set to select the inputs, output format, and the various color controls, as follows:

a) To receive the color difference signals at Pins 30 and 31, along with the selected luma input, set bit $80–7 = 1. The RGB inputs will be disabled. Select the luma input with bits $81–7 and $81–6.
b) To receive the RGB signals at Pins 26 to 28, set bit $80–7 = 0, and the FC input (Pin 25) at a logic high. In this condition, the color difference inputs and the luma signals will be disabled.
c) When RGB signals are selected, internally they may take one of two paths:
   – Setting bit $82–6 = 0 provides brightness and contrast controls, but not saturation.
   – Setting bit $82–6 = 1 provides for saturation control, as well as brightness and contrast.
d) The output format, RGB or YUV, is set with bit $82–7. If the bit is 0, RGB is selected, and the DACs of registers $7D and $7E must be set to 0. If YUV is selected ($82–7 = 1), those two DACs must be set to 32 (midpoint). The YUV format cannot be selected if the RGB inputs are selected, and bit $82–6 = 0.
e) The color controls in this section are seven, controlled via 6–bit DACs in subregisters $80 – $86. They are as follows:

DAC	Function	Suggested Value
$81–5/0	Main Contrast	47
$84–5/0	Main Brightness	30
$86–5/0	Saturation	32
$80–5/0	Blue Contrast Trim	32
$82–5/0	Red Contrast Trim	32
$83–5/0	Blue Brightness Trim	32
$85–5/0	Red Brightness Trim	32

The first three registers mentioned above are main controls for the outputs, while the last four are for fine tuning. Note that the saturation control listed above is in addition to the saturation control in the decoder, mentioned earlier in this document. See Table 8 in the MC44011 data sheet for a description of the color controls. The suggested values above are starting points only, and may have to be adjusted for the specific application.

PIXEL CLOCK GENERATOR

This section produces a pixel clock, intended for use by a subsequent A/D, which has a frequency that is a direct multiple of the horizontal frequency. The direct multiple value is determined by the divider ratio of the external frequency divider between Pins 15 and 18. In other words:

Pixel Clock Frequency = Horizontal Frequency x Divider Ratio

Before this section can operate properly, the horizontal PLL must be locked up and stable with respect to the incoming video.

The pixel clock output (Pin 18) does not have a great deal of drive capability, and must be handled carefully to keep jitter down. Loading on this pin should generally not exceed two LSTTL loads, and the less the better. The suggested divider shown in Figure 46 of the MC44011 data sheet shows 3F type TTL loads, and functions satisfactorily. The PC board trace from Pin 18 to the divider and the A/D should be kept short. Check the waveform at Pin 18 with a scope (the probe must have its own ground connection). If it is rounded off, there is too much loading on the pin, and this will contribute to jitter. See Figure 7 for an example of the pixel clock at 13.5 MHz, using the circuit in Figure 46 of the MC44011 data sheet.

The return signal to Pin 15 must be an active low TTL pulse with a low time greater than 200 ns, and less than 45 μs. See Figure 32 in the MC44011 data sheet.

If the pixel clock frequency is to be 22 MHz or higher, the divide–by–two should be de–selected (bit $85–7 = 0). If the frequency is to be less than 22 MHz, then bit $85–7 should be set to a 1. Then set the DAC of register $7F to its midpoint (10 0000 or 32_d), and set bit $83–7 to a 1 (low gain). This will set the gain of the pixel clock VCO in a usable range. Check flags 19 and 20 – they must both be 0. If either one is a 1, then change the value of the $7F DAC up or down until both flags are 0. If the DAC ends up being set close to the high end

t(above 45), then change bit $83–7 to a 0 (high gain), and it should be possible to lower the value of the $7F DAC. If the $7F DAC is set above 50, the pixel clock will usually be unstable. The best combination of this DAC and the gain bit must be found by trial and error, as they depend on:

– The specific pixel clock frequency
– The characteristics of the divider
– The PC board layout

Generally the best values for the DAC are towards the low end (<32). In addition, the gain of the horizontal PLL ($83–6) can affect the pixel clock.

If a good setting for the gain bit and the DAC cannot be found, check that the components at Pin 16 are correct, and also the characteristics of the divider for jitter. The waveform at Pin 16 is a flat dc signal, at a value between 1.5 V and 3.5 V. The exact voltage depends on the frequency, and the gain setting.

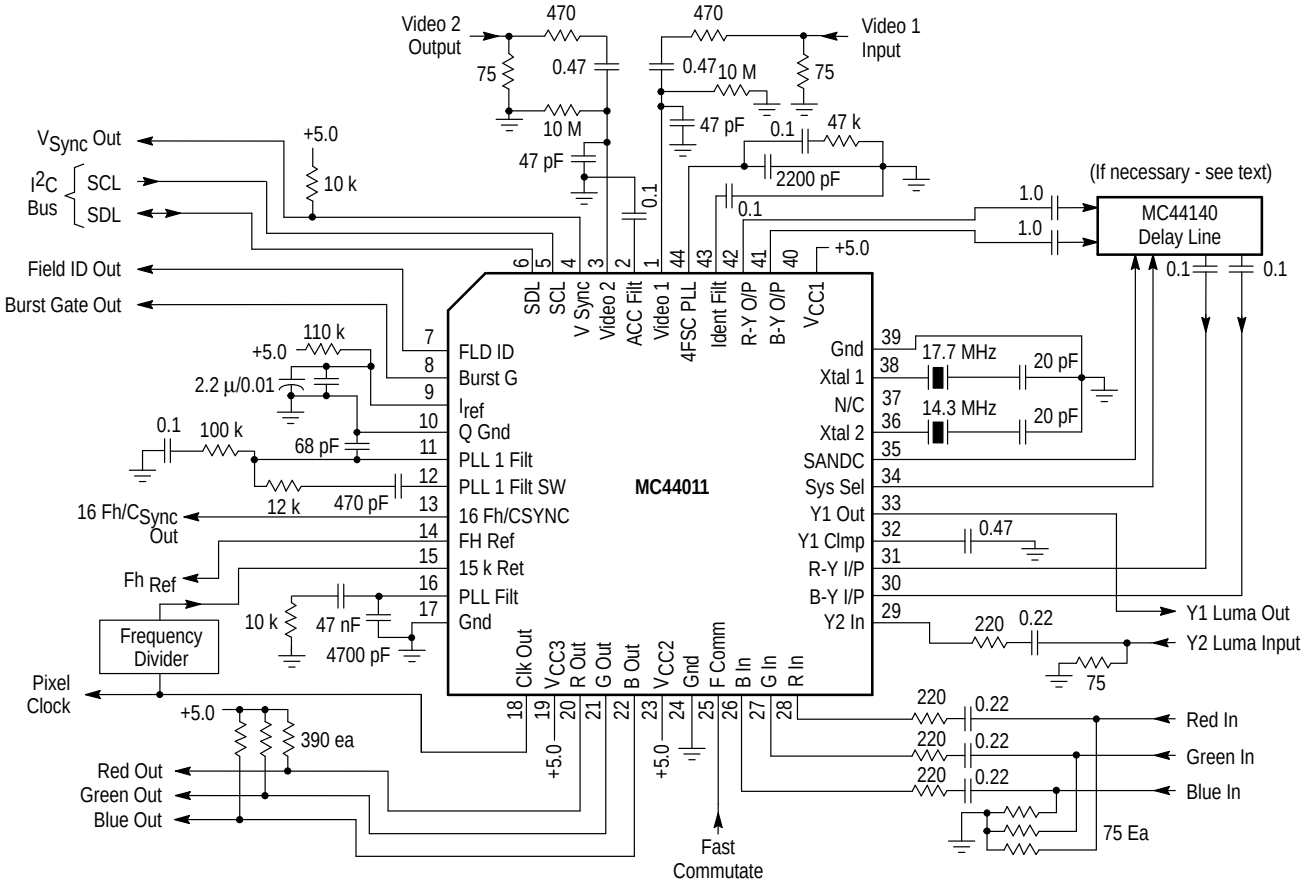
The only limitation on the use of the pixel clock generator is that if its frequency is to be within 1.0 MHz of the selected crystal (or 2x the crystal frequency), unacceptable artifacts and patterning may result on the RGB outputs and on the screen. The closer the pixel clock frequency is to the crystal frequency, the stronger the artifacts. Acceptance or rejection of the artifacts must be determined for each application. If they are deemed unacceptable, then this section should be disabled (set the $7F DAC to 63, and/or ground Pin 16), and use the MC44145 instead. The MC44145 has the same pixel clock generator circuit as the MC44011, but by being external, the interference within the MC44011 will not occur.

The ultimate test of the adjustment and operation of the pixel clock is, of course, the quality of the video as viewed on the screen of the final product.

CONCLUSION

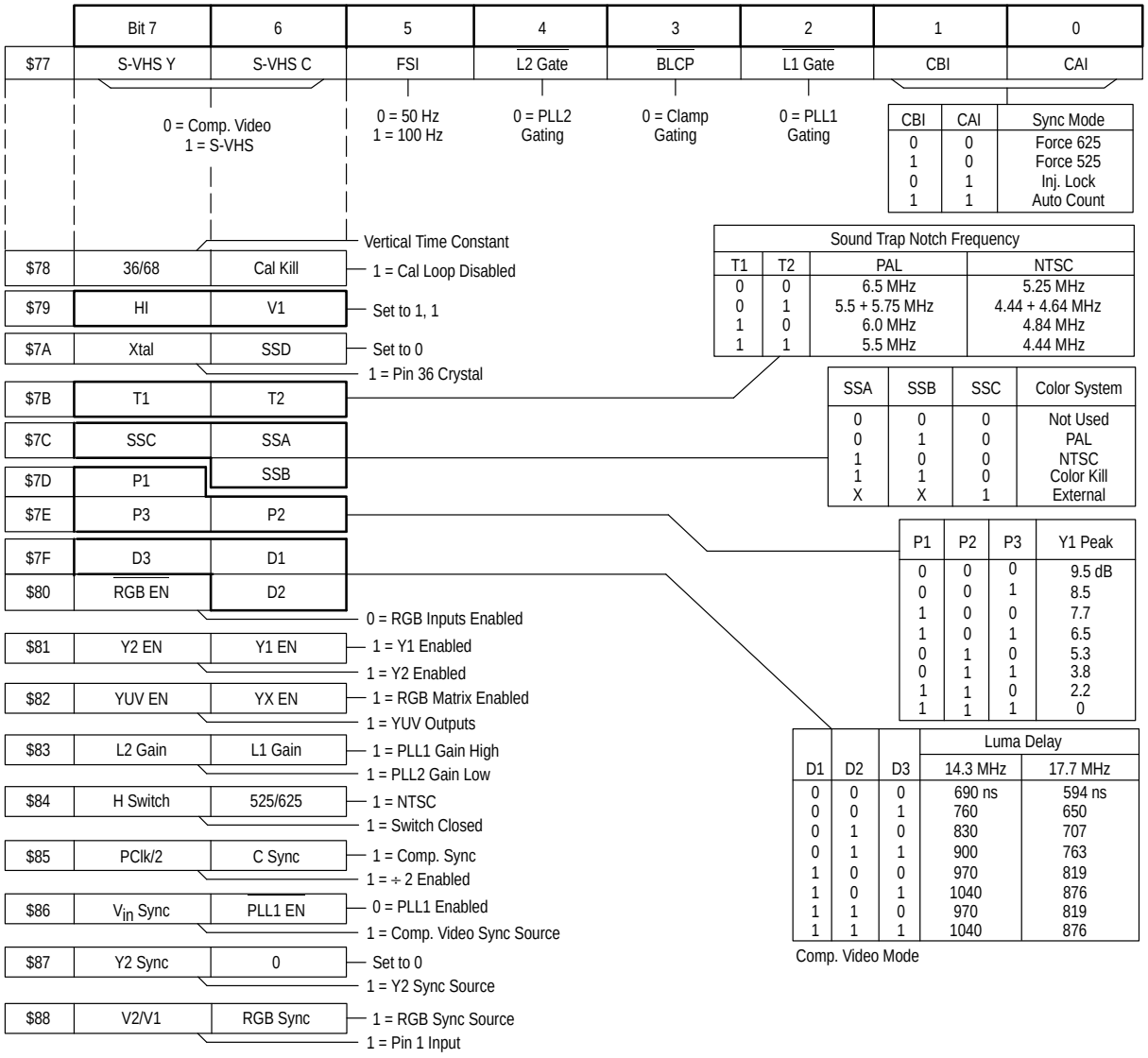
That's it! All sections of the MC44011 have been covered. Hopefully this application note has helped clarify, as well as expand on, the information in the data sheet. But if there are additional questions about the operation of this part, please call the nearest Motorola sales office for applications assistance.

Figure 1. Basic Application Circuit



The above circuit is the basic circuit for the MC44011. All available inputs and outputs are indicated, although they may not all be used in each application. Please refer to the MC44011 data sheet for details on the Frequency Divider, and for connecting the MC44140 delay line.

APPENDIX A – CONTROL BIT SUMMARY



CBI	CAI	Sync Mode
0	0	Force 625
1	0	Force 525
0	1	Inj. Lock
1	1	Auto Count

Sound Trap Notch Frequency			
T1	T2	PAL	NTSC
0	0	6.5 MHz	5.25 MHz
0	1	5.5 + 5.75 MHz	4.44 + 4.64 MHz
1	0	6.0 MHz	4.84 MHz
1	1	5.5 MHz	4.44 MHz

SSA	SSB	SSC	Color System
0	0	0	Not Used
0	1	0	PAL
1	0	0	NTSC
1	1	0	Color Kill
X	X	1	External

P1	P2	P3	Y1 Peak
0	0	0	9.5 dB
0	0	1	8.5
1	0	0	7.7
1	0	1	6.5
0	1	0	5.3
0	1	1	3.8
1	1	0	2.2
1	1	1	0

			Luma Delay	
D1	D2	D3	14.3 MHz	17.7 MHz
0	0	0	690 ns	594 ns
0	0	1	760	650
0	1	0	830	707
0	1	1	900	763
1	0	0	970	819
1	0	1	1040	876
1	1	0	970	819
1	1	1	1040	876

Comp. Video Mode

Control DACs

$78	R-Y/B-Y Gain Adjustment	$82	Red Contrast Trim
$79	Subcarrier Phase	$83	Blue Brightness Trim
$7D	Blue DC Bias	$84	Main Brightness
$7E	Red DC Bias	$85	Red Brightness Trim
$7F	Pixel Clock VCO Gain	$86	Saturation (Color Diff. Section)
$80	Blue Contrast Trim	$87	Saturation (Decoder)
$81	Main Contrast	$88	Hue

Flags

10	Internally Set to 1	19	Pixel Clock VCO Gain too low
11	Horizontal Loop (PLL1) Enabled	20	Pixel Clock VCO Gain too high
12	Horizontal Loop not Locked	21	Internally Set to 1
13	Internally Set to 0	22	Internally Set to 0
14	Less than 576 Lines	23	ACC Loop Active
15	Vertical Decoder Engaged	24	PAL Signals Detected
16	Internally Set to 1	25	Not Used
17	Internally Set to 1	26	Internally Set to 0

APPENDIX B – CRYSTAL INFORMATION

Table 1. Crystal Specifications

Frequency: (4 x subcarrier)	NTSC: 14.31818 MHz PAL: 17.734472 MHz PAL–M: 14.30244 MHz
Pull–in range:	±1600 Hz (with respect to crystal frequency)
Tolerance:	30 ppm (with fixed load capacitor)
Temperature Coefficient:	50 ppm (with fixed load capacitor)
Operating Mode:	Fundamental, series resonance
Load Capacitance:	Nominally 20 pF
Motional Capacitance:	10 to 30 fF
Series Resistance:	<30 Ω (nominally 10 Ω)

The following sources can be used to obtain the crystals:

Standard Crystals Corp. (818–443–2121)
9940 E. Baldwin Pl.
El Monte, CA 91731
Example: “17.734472 MHz Fundamental Crystal, 20 pF load, 0.001% tolerance, HC–49 Case style.”

International Crystal Mfg. Co., Inc. (405–236–3741)
701 W. Sheridan
Oklahoma City, OK 73126–0330
Example: “Group B medium frequency crystal, # 434263, 14.31818 MHz.” (This specifies a crystal calibrated at 26°C, 25 ppm tolerance, FM–1 case (similar to HC–49), and a 20 pF load.)

Motorola does not endorse or warrant the suppliers mentioned above.

Figure 2. Burst Gate Output (Pin 8)

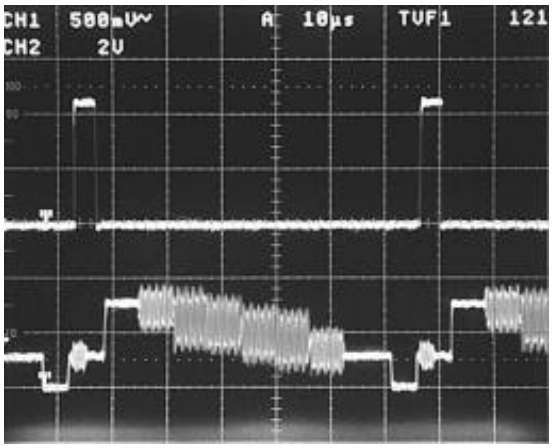
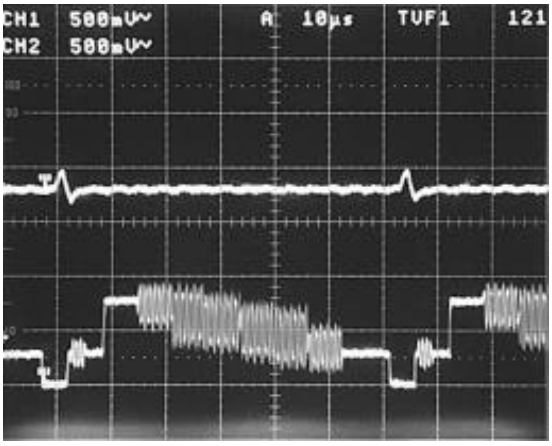


Figure 3. Horizontal PLL Filter (Pin 11)



NOTE: The lower trace in the above photos is the scope’s channel 1, and is the input at Pin 1 – NTSC color bars. The upper trace (channel 2) is the indicated output.

Figure 4. Incorrectly Locked Vertical Sync Output (Pin 4)

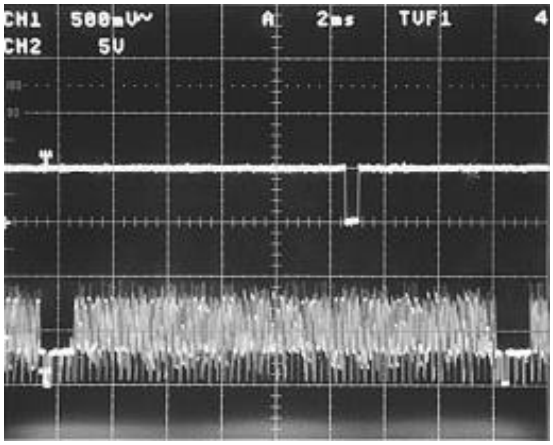
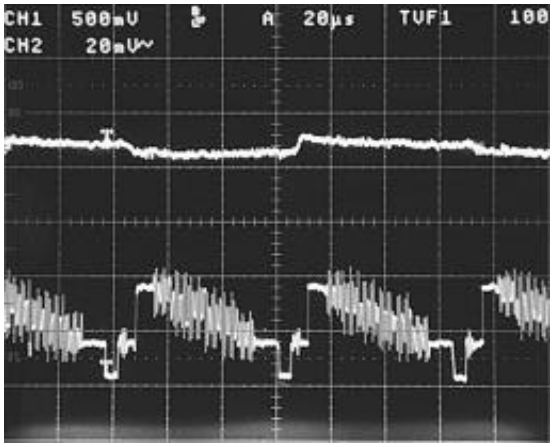


Figure 5. Crystal PLL Filter with NTSC Signal (Pin 44)



NOTE: The lower trace in the above photos is the scope's channel 1, and is the input at Pin 1 – NTSC color bars. The upper trace (channel 2) is the indicated output.

Figure 6. Crystal PLL Filter with PAL Signal (Pin 44)

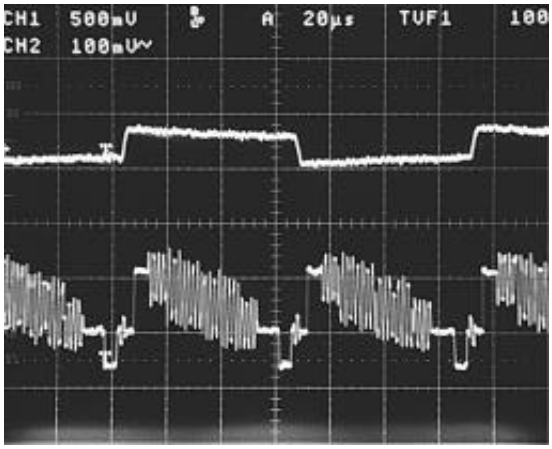
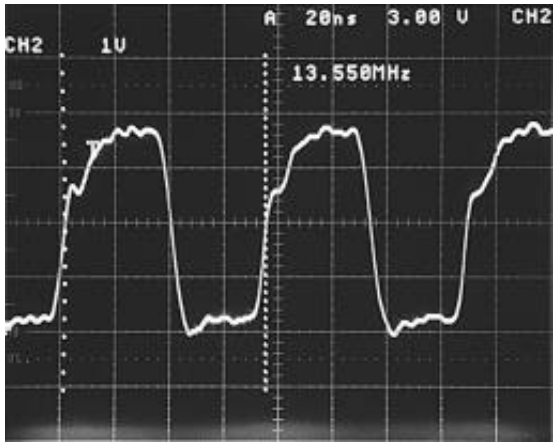


Figure 7. Pixel Clock Output (Pin 18)



NOTE: The lower trace in the above photo is the scope's channel 1, and is the input at Pin 1 – PAL color bars. The upper trace (channel 2) is the indicated output.

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