Order this document by AN1537/D

AN1537
Application Note

MC10SX1189 I/O SPICE Modelling Kit

Prepared by
Bernie Weir
Applications Engineering

This application note provides the SPICE information necessary to accurately model system interconnect situations for designs which utilize the MC10SX1189 Fibre Channel Coaxial Cable Driver and Loop Resiliency Circuit.

2/95

REV 0

MOTOROLA

MC10SX1189 I/O SPICE Modelling Kit

OBJECTIVE

The objective of this kit is to provide customers with enough circuit schematic and SPICE parameter information to allow them to perform system level interconnect modelling for the MC10SX1189 Fibre Channel Coaxial Cable Driver and Loop Resiliency Circuit. This product is realized using the MOSAIC III bipolar process which is used in Motorola's family of high performance ECL; ECLinPS and ECLinPS Lite.

The kit contains representative schematics for the different high speed I/O circuits used in the MC10SX1189. In addition a worst case package model schematic is included for more accurate system level modelling. The package model represents the parasitics as they are seen on a corner pin, which is the worst case condition for the SOIC 16. If more typical values are desired a 20% reduction in the capacitance and the inductance of the package model can be used. This package model should be placed on all external inputs to the input gates, all outputs of the output gates and on the V_{CC} line. If desired the model can also be placed on the GND line, however this is not necessary due to the static nature of GND.

There is only one schematic, Figure 1, to represent the input structure of the device. There are two basic output structures needed to model the device. The structure in Figure 2 represents the normal PECL output circuitry (QR) and is intended to drive a 50 Ω transmission line. Figures 3 represents the enhanced double amplitude output (QT) used to interface to the cable or printed circuit transmission line.

To support the wide bandwidth requirements of full rate 1063 MBaud/s data streams, the outputs have been enhanced by using higher current levels in the output buffers. This added current allows the parasitic capacitances of the gate to charge and discharge more quickly, thus enhancing the transition time performance of the device.

The package model is found in Figure 4 and the ESD circuitry is in Figure 5. The ESD structure should be added to both the inputs and outputs. Finally the package model should be included on all input and output pins and at least the V_{CC} power supply.

SPICE Parameter Information

In addition to the schematics, a listing of the SPICE parameters for the transistors referenced in the schematics is included. These parameters represent a typical device of the given transistor size. Varying these parameters will obviously affect the voltage levels, the propagation delays, and the transition times of a device. For the type of modelling for which this information is intended, the actual propagation delay of a device will not be modelled, as a result variations in this parameter are meaningless. Furthermore the voltage levels and transition times can be more easily varied by other means. This will be addressed in the next section.

All of the resistors referenced in the schematics are polysilicon resistors and thus there is no need to provide parasitic capacitance models for these resistors in the netlist. The only devices needed in the SPICE netlist are illustrated in the schematics.

Modelling Information

The bias driver schematics are not included as they were deemed unnecessary for interconnect simulation, in addition their use also results in a relatively large increase in simulation time. Alternatively the internal reference voltages (V_{BB} and V_{CLAMP}) should be driven with ideal constant voltage sources. The following table summarizes the voltage levels for these internal references as well typical input voltage parameters. It is important to note that V_{BB}, V_{IL}, and V_{IH} track directly with variations in V_{CC} so the tables below assume that V_{CC} = 5.0V. The relationship is noted next to the typical vaue.

Parameter	Typical Level	Worst Case
V_{BB}	3.625V (V_{CC} – 1.375)	Data Book
V_{CS}	1.33V	±50mV
CLAMP	2.2V	±50mV
V_{IH}	4.1V (V_{CC} – 0.9V)	Data Book
V_{IL}	3.25V (V_{CC} –1.75V)	Data Book
Rise/Fall	300ps (20% – 80%)	

The schematics and SPICE parameters provided will provide a somewhat typical output waveshape which may not represent the worst case system situation. Fortunately there are some simple adjustments that can be made to the schematics to provide output characteristics at or near the corners of the data book specification limits. First to adjust the V_{OH} level one simply needs to lower the V_{CC} value by the amount one wishes to alter the V_{OH} level. This V_{CC} adjustment will obviously also result in a change in the V_{OL} level. To change the V_{OL} level independent of the V_{OH} level the collector load resistors can be increased or decreased depending on the change desired (Note: V_{OH} will change slightly due the the I_bR drop portion of the V_{OH} level). The V_{OL} can also be changed by increasing/decreasing the current in the gate via the current source resistor. In addition to changing the V_{OL} level, by increasing/decreasing the gate current the output rise and fall times will decrease/increase due to the additional current available to charge and discharge the stray capacitance on the collectors of the output differential pair. If the user would like to adjust the levels and transition times of an output gate to represent a corner of the guaranteed specification the following sequence should be followed:

1) Adjust the gate current to produce the desired output slew rate
2) Adjust the V_{CC} for the desired V_{OH}
3) Adjust the collector load resistor for the desired V_{OL}

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling.

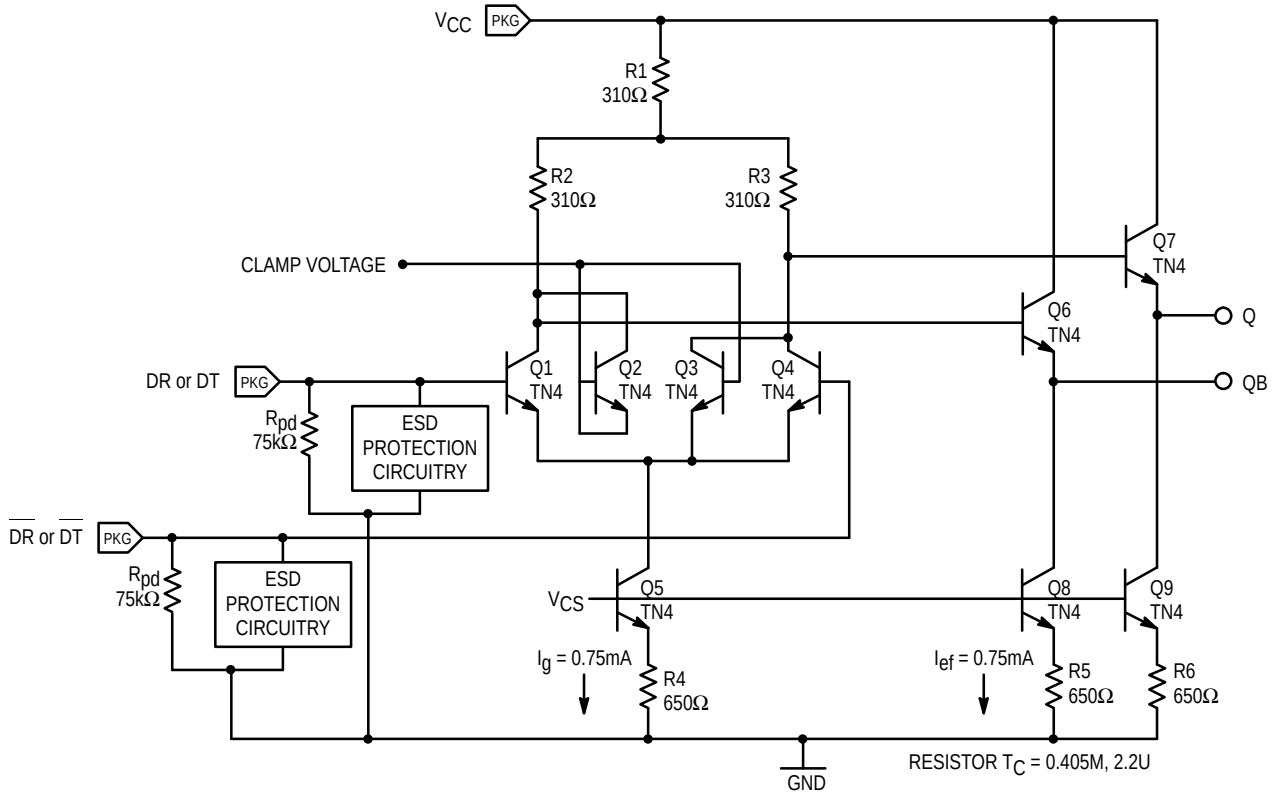

Figure 1. Simplified Input Schematic

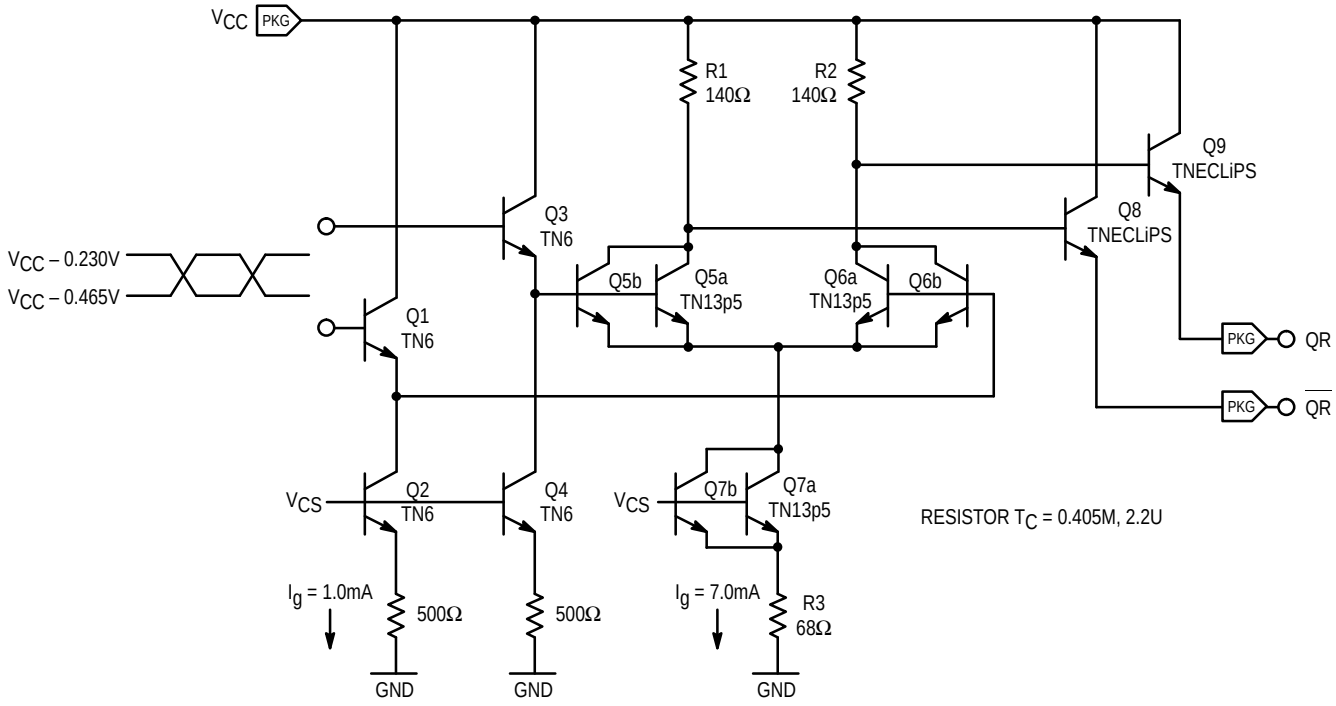

Figure 2. Simplified Normal PECL Swing Output Schematic

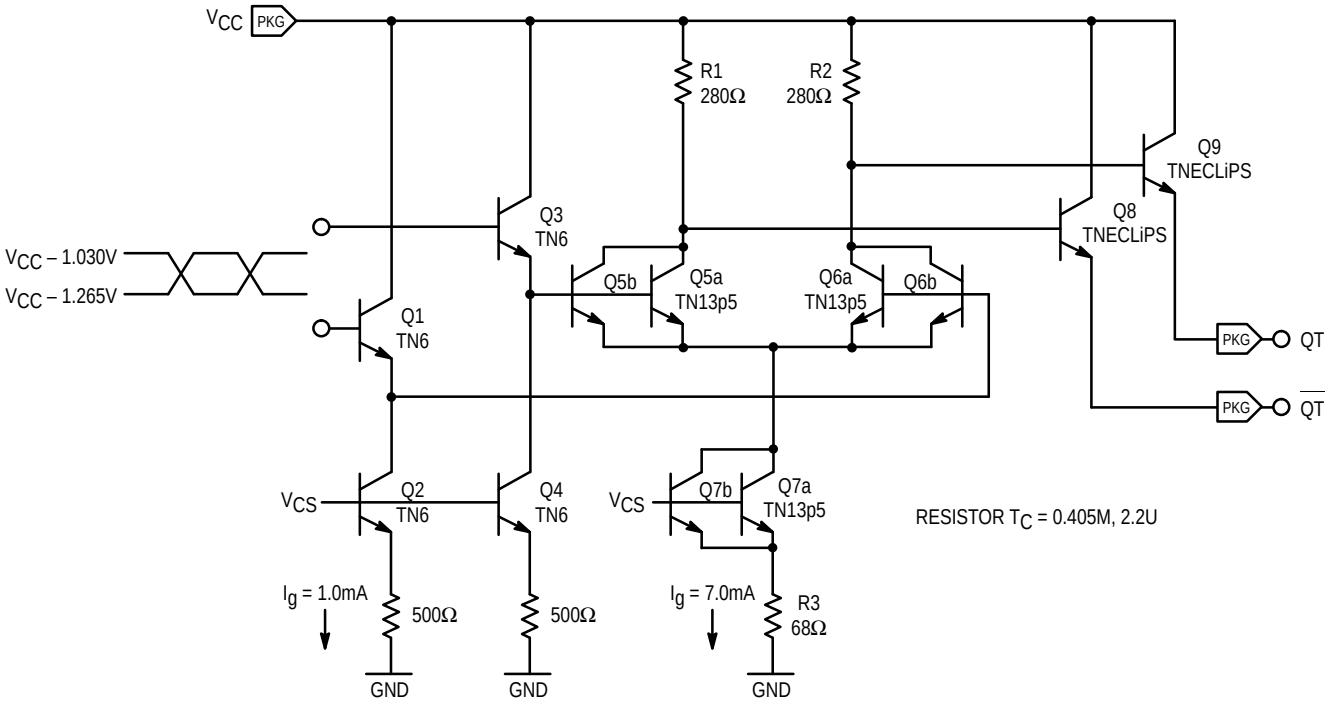

Figure 3. Simplified Enhanced Swing Output Schematic

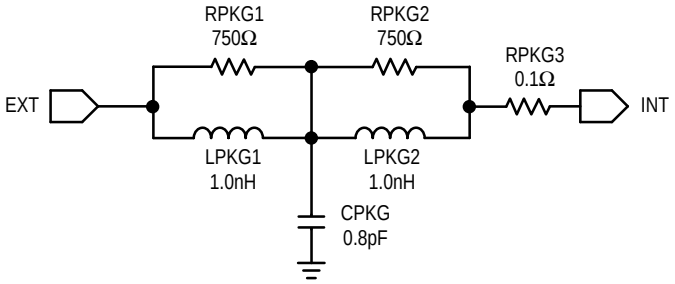

Figure 4. Package Model Schematic

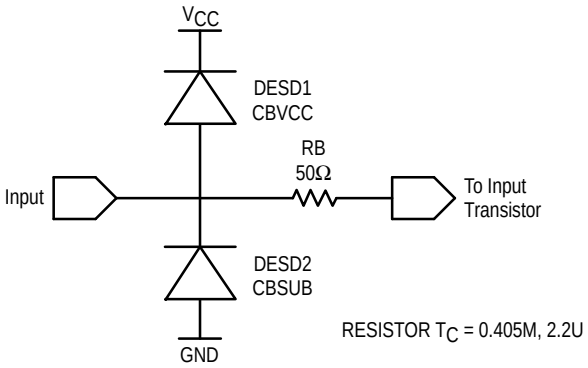

Figure 5. ESD Protection Circuitry

APPENDIX

SPICE Transistor Model Parameters

```
**** 1.75u x 4.0u emitter
.MODEL TN4          NPN
+ ( IS= 5.27E–18   BF=120   NF=1   VAF=30   IKF=6.48mA
+   ISE= 2.75E–16 BR=10    NE=2   VAR=5    IKR=567uA
+   IRB= 8.1uA     RB= 461.6  RBM= 142.5  RE= 21.6  RC= 83.1
+   CJE= 19.9fF    VJE= .9    MJE= .4            XTB= 0.73
+   CJC= 25.1fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 49.6fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS        TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 17.0mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*

**** 1.75u x 6.0u emitter
.MODEL TN6          NPN
+ ( IS= 8.56E–18   BF=120   NF=1   VAF=30   IKF=10.5mA
+   ISE= 4.48E–16 BR=10    NE=2   VAR=5    IKR=922uA
+   IRB= 13.2uA     RB= 291.4  RBM= 95.0  RE= 13.3  RC= 62.7
+   CJE= 29.9fF    VJE= .9    MJE= .4            XTB= 0.73
+   CJC= 31.2fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 60.9fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS        TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 27.6mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*

**** 1.75u x 13.5u emitter
.MODEL TN13P5          NPN
+ ( IS= 2.09E–17   BF=120   NF=1   VAF=30   IKF=25.7mA
+   ISE= 1.09E–15 BR=10    NE=2   VAR=5    IKR=2.25mA
+   IRB= 32.2uA     RB= 122.6  RBM= 42.2  RE= 5.44  RC= 32.8
+   CJE= 67.4fF    VJE= .9    MJE= .4            XTB= 0.73
+   CJC= 53.8fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 103fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS        TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 67.5mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*

**** ESD Diode
.MODEL CBVCC D
+ (IS= 1.00E–15  CJO= 527fF  Vj= 0.545  M= 0.32  BV= 14.5  IBV= 0.1E–6
+ XTI= 5  TT=1nS)
*

**** Output Emitter Follower
.MODEL TNECLIPS          NPN
+ ( IS= 2.27E–16   BF=120   NF=1   VAF=30   IKF=279mA
+   ISE= 1.19E–14 BR=10    NE=2   VAR=5    IKR=24.4mA
+   IRB= 349uA     RB= 15.98  RBM= 4.17  RE= .501  RC= 11.1
+   CJE= 611fF    VJE= .9    MJE= .4            XTB= 0.73
+   CJC= 440fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 668fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS        TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 733mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*
```

```
**** Output Emitter Follower
.MODEL TNECLIPS          NPN
+ ( IS= 2.27E–16   BF=120   NF=1   VAF=30   IKF=279mA
+   ISE= 1.19E–14 BR=10     NE=2   VAR=5     IKR=24.4mA
+   IRB= 349uA      RB= 15.98  RBM= 4.17  RE= .501  RC= 11.1
+   CJE= 611fF    VJE= .9     MJE= .4              XTB= 0.73
+   CJC= 440fF    VJC= .67  MJC= .32             XCJC= .3
+   CJS= 668fF    VJS= .6    MJS= .4             FC= .9
+   TF= 8pS         TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 733mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
```


Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.