AN1503
Application Note

ECLinPS™ I/O SPICE Modelling Kit

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This application note provides the SPICE information necessary to accurately model system interconnect situations for high speed ECLinPS designs. The note includes information on both the standard ECLinPS family, as well as the ECLinPS Lite products.

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ECLinPS I/O SPICE Modelling Kit

Objective

The objective of this kit is to provide customers with enough circuit schematic and SPICE parameter information to allow them to perform system level interconnect modelling for the Motorola ECLinPS and ECLinPS Lite logic families. The ECLinPS and ECLinPS Lite families are Motorola's highest performance ECL families. With packaged gate delays of 300ps and output edge rates as low as 175ps these two families define the state-of-the-art in ECL logic. This kit is not intended to provide the user with the information necessary to perform extensive device modelling for any particular ECLinPS or ECLinPS Lite device. If users wish to perform the latter type of SPICE modelling they are encouraged to contact an ECLinPS Applications Engineer to obtain more detailed schematics and SPICE parameter information.

Schematic Information

The kit contains representative schematics for the different I/O circuits used in the ECLinPS and ECLinPS Lite families. In addition a worst case package model schematic is included for more accurate system level modelling. The package model represents the parasitics as they are seen on a corner pin, a sizable distance from an AC ground. If more typical values are desired a 20% reduction in the capacitance and the inductance of the package model can be used. This package model should be placed on all external inputs to the input gates, all outputs of the output gates and on the V_{CC} line. If desired the model can also be placed on the V_{EE} line, however this is not necessary due to the static nature of V_{EE}.

There is only one schematic, Figure 1, to represent the input structures of the family. For interconnect purposes this one schematic will adequately represent all of the ECLinPS devices except the differential input devices and the simple gates. The schematic in Figure 1 can be modified to represent differential devices by simply adding the package model and the ESD structure to the "V_{BB}" input and using this as the inverted signal input. For the simple gates the input gate is actually the output gate represented by Figure 2. Therefore these devices should be modelled with the circuit of Figure 2 with the appropriate package model and ESD circuitry from Figure 1 added to the schematic. For the devices in the ECLinPS Lite family outlined in the appendix whose output and input buffers are one in the same the ESD circuitry and package models should be added to the appropriate output buffer. A list of devices which incorporate this structure is included in the appendix of this document.

There are five basic output structures needed to represent both families. The structure in Figure 2 mentioned above represents the structure used in the majority of the family, a simple 50Ω drive output cell. Figures 3 and 4 represent the special output functions used in the ECLinPS and ECLinPS Lite families. Figure 3 shows the circuit configuration for a multiple output device (ie E112). Notice the doubling of the gate current necessary to drive the multiple output emitter followers. Figure 4 is the typical bidirectional 25Ω output structure used for the two bus driving functions currently in the ECLinPS family. Notice the doubled output emitter follower (OEF). This is necessary to provide a small enough V_{BE} to produce an acceptable V_{OH} level while providing the current necessary for 25Ω drive. In addition the collector load resistors have been increased to provide a cutoff V_{OL}. Due to the larger collector load resistor the gate current is increased 3x to reduce the relative size of the collector load resistors so that the I_b of the OEF does not produce an I_R drop across the collector load resistor sufficient to create a marginal V_{OH}.

The schematics in Figures 5 and 6 represent the bandwidth enhanced ECLinPS and ECLinPS Lite devices. Because the bandwidth of standard ECLinPS devices are limited by their rise and fall times, the bandwidth can be enhanced by simply using higher current levels in the output buffers. This added current allows the parasitic capacitances of the gate to charge and discharge more quickly, thus enhancing the transition time performance of the device. Thus far two levels of gate current increase have been used to reach two different plateaus of performance. The majority of the enhanced bandwidth ECLinPS and ECLinPS Lite devices utilize the 2x current increase of Figure 4. A full outline of the devices which utilize these buffers can be found in the appendix.

The schematics of Figure 7 represent the temperature compensation networks present in the output structures for 100E devices. The output buffer schematics all reference one of the temperature compensation networks. The temperature compensation circuitry should be placed as pictured in the output buffer schematics with L and R representing left and right of the schematic. Obviously for 10E circuit outputs these networks can be ignored. Also included in the appendix is the package model of Figure 8 and the ESD circuitry of Figure 9. The ECLinPS ESD should be added to any input of an ECLinPS device being driven by a signal off chip. The ECLinPS Lite ESD should be added to both the inputs and outputs for any ECLinPS Lite device being modelled. Finally the appropriate package model (8–lead SOIC for ECLinPS Lite or 28–lead PLCC for ECLinPS) should be included on all input and output pins and at least the V_{CC} power supply.

Both the typical and multiple output circuits show differential inputs and outputs. If the user is simulating a single ended device the OEF and associated package model and load resistor of the unneeded output should be deleted from the schematic. If the user chooses to drive an output cell directly instead of using the input cell either of the following two driving approaches can be used:

	IN	V_{BB}	Rise/Fall
Diff	–1.2V > –1.6V	–1.6V > –1.2V	180ps (20% – 80%)
S.E.	–0.9V > –1.75V	–1.325V	180ps (20% – 80%)

SPICE Parameter Information

In addition to the schematics a listing of the SPICE parameters for the transistors referenced in the schematics is included. These parameters represent a typical device of the given transistor size. Varying these parameters will obviously affect the voltage levels, the propagation delays, and the transition times of a device. For the type of modelling for which this information is intended the actual propagation delay of a device will not be modelled, as a result variations in this parameter are meaningless. Furthermore the voltage levels and transition times can be more easily varied by other means. This will be addressed in the next section.

All of the resistors referenced in the schematics are polysilicon resistors and thus there is no need to provide parasitic capacitance models for these resistors in the netlist. The only devices needed in the SPICE netlist are illustrated in the schematics.

Modelling Information

The bias driver schematics are not included as they were deemed unnecessary for interconnect simulation, in addition their use also results in a relatively large increase in simulation time. Alternatively the internal reference voltages (V_{BB} and V_{CS}) should be driven with ideal constant voltage sources. The following table summarizes the voltage levels for these internal references as well typical input voltage parameters.

Parameter	Typical Level	Worst Case
V_{BB}	–1.325V	Data Book
V_{CS}	V_{EE} + 1.33V	±50mV
V_{IH}	–0.9V (10E); –0.95V (100E)	Data Book
V_{IL}	–1.75V (10E); –1.7V (100E)	Data Book
Rise/Fall	400ps (20% – 80%)	Data Book

The schematics and SPICE parameters provided will provide a somewhat typical output waveshape which may not represent the worst case system situation. Fortunately there are some simple adjustments that can be made to the schematics to provide output characteristics at or near the corners of the data book specification limits. First to adjust the V_{OH} level one simply needs to lower the V_{CC} value below ground by the amount one wishes to alter the V_{OH} level. This V_{CC} adjustment will obviously also result in a change in the V_{OL} level. To change the V_{OL} level independent of the V_{OH} level the collector load resistors can be increased or decreased depending on the change desired (Note: V_{OH} will change slightly due the the I_bR drop portion of the V_{OH} level). The V_{OL} can also be changed by increasing/decreasing the current in the gate via the current source resistor. In addition to changing the V_{OL} level, by increasing/decreasing the gate current the output rise and fall times will decrease/increase due to the additional current available to charge and discharge the stray capacitance on the collectors of the output differential pair. If the user would like to adjust the levels and transition times of an output gate to represent a corner of the guaranteed specification the following sequence should be followed:

1) Adjust the gate current to produce the desired output slew rate
2) Adjust the V_{CC} for the desired V_{OH}
3) Adjust the collector load resistor for the desired V_{OL}

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling. The block diagram of Figure 10 illustrates the type of situation which can be effectively modelled using the ECLinPS I/O SPICE Modelling Kit. The schematic information provided in this document is available in netlist form through EMAIL or an IBM or Macintosh disk, although with today's advanced design tools it will probably be a simpler task to enter the schematics in a good schematic capture package than it would be to manipulate the generic netlist. If however the netlist are desired, clarification is needed or additional information is necessary the user is encourage to contact any ECLinPS Application Engineering personnel for assistance.

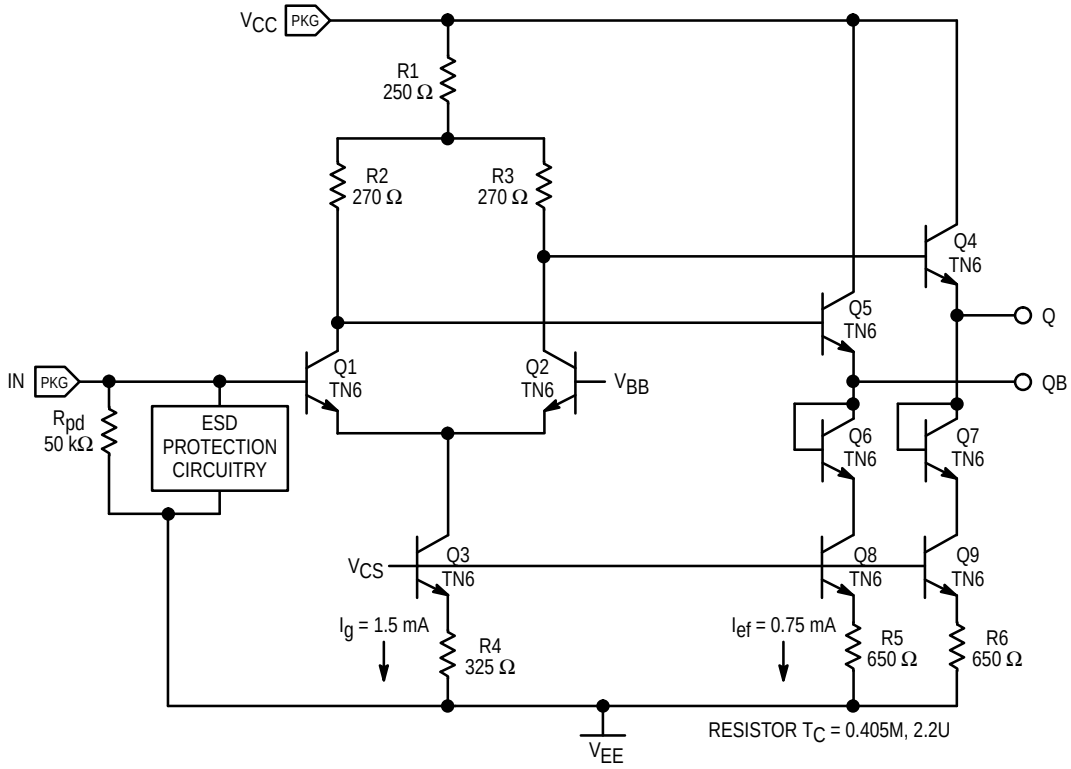

Figure 1. Typical Input Schematic

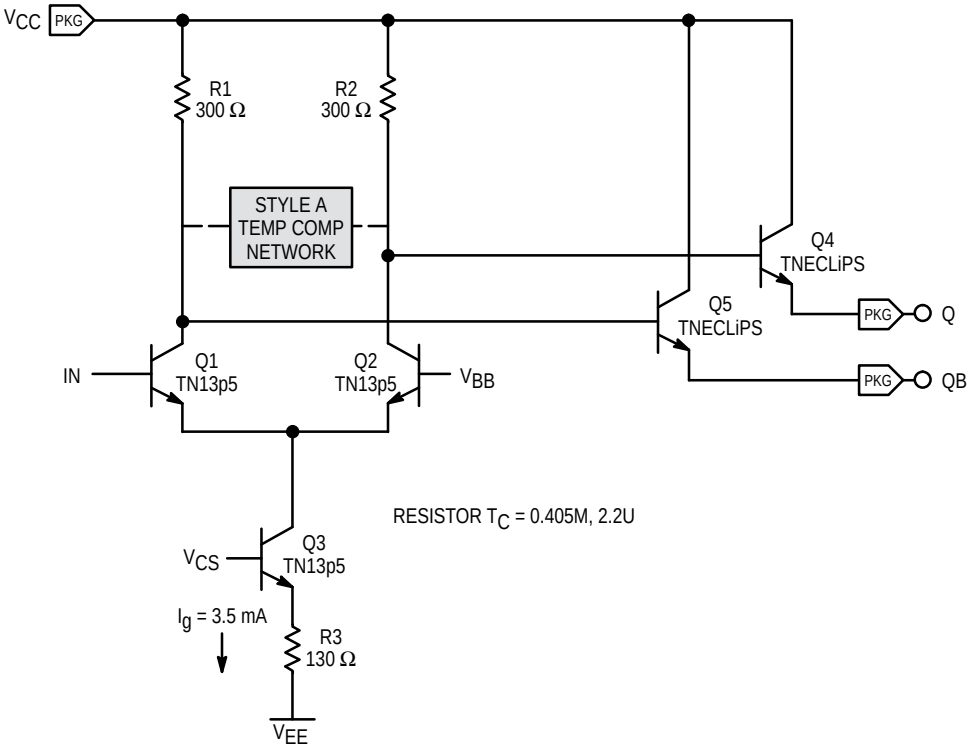

Figure 2. Typical Output Schematic

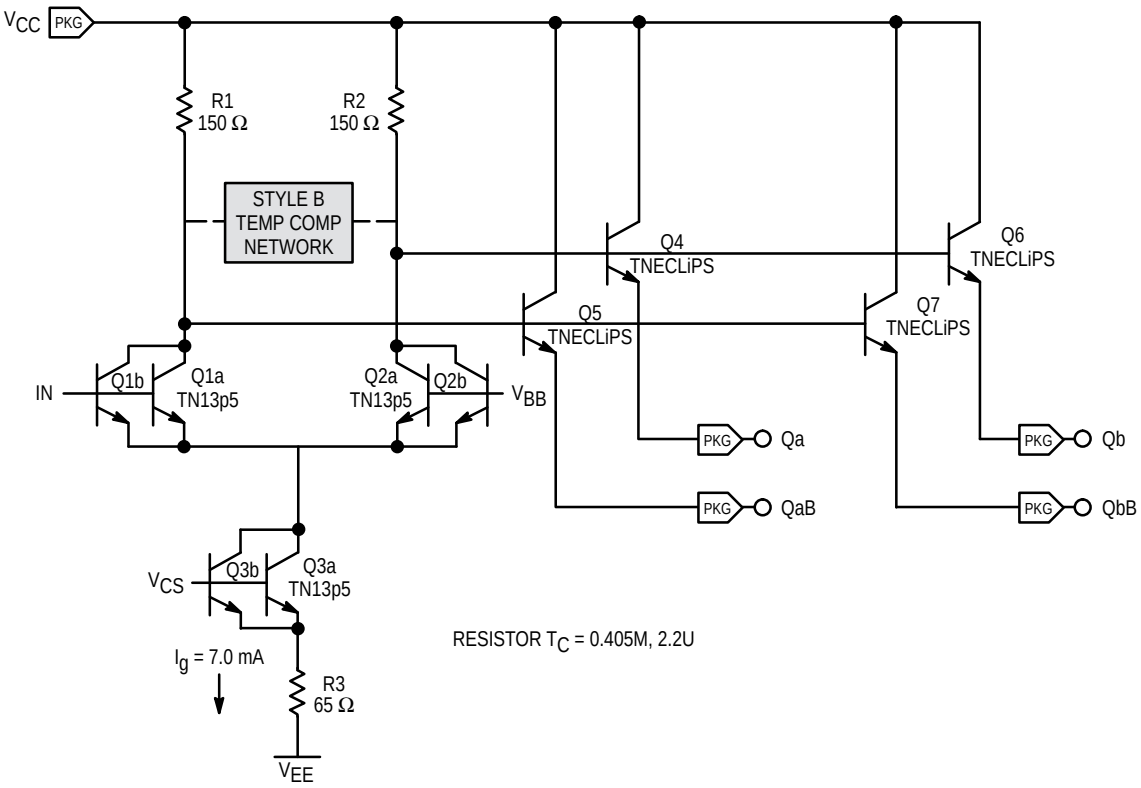

Figure 3. Multiple Output Schematic

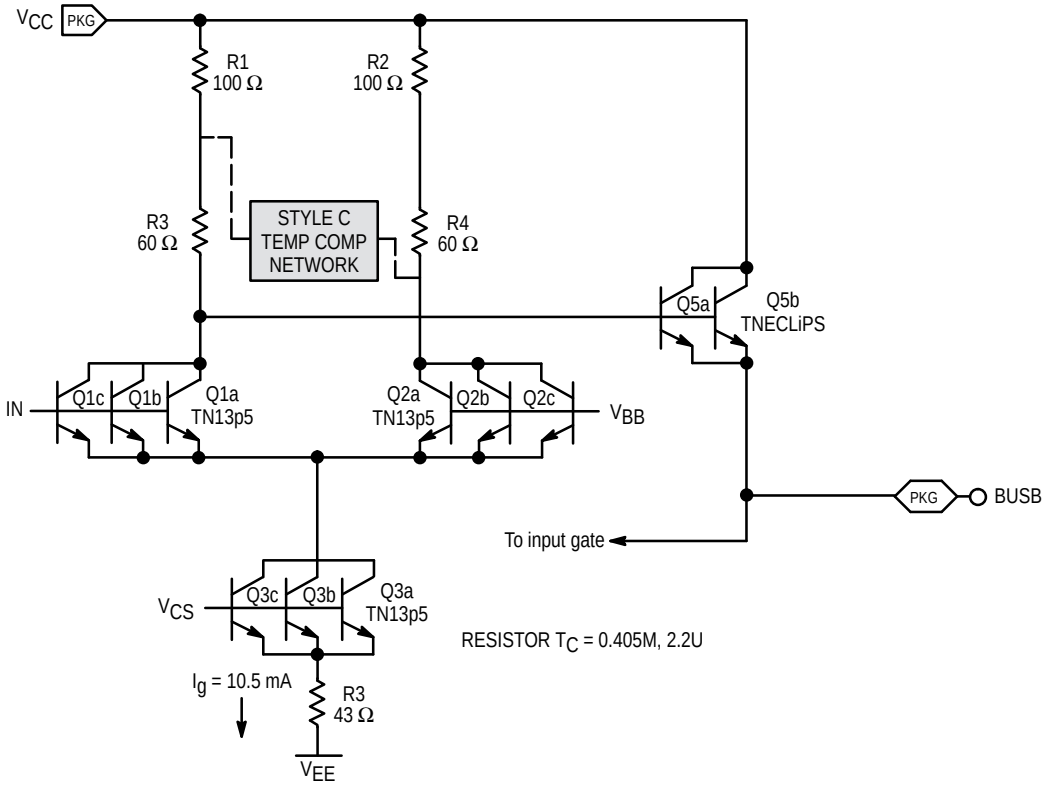

Figure 4. 25 Ω Bus Driver Output

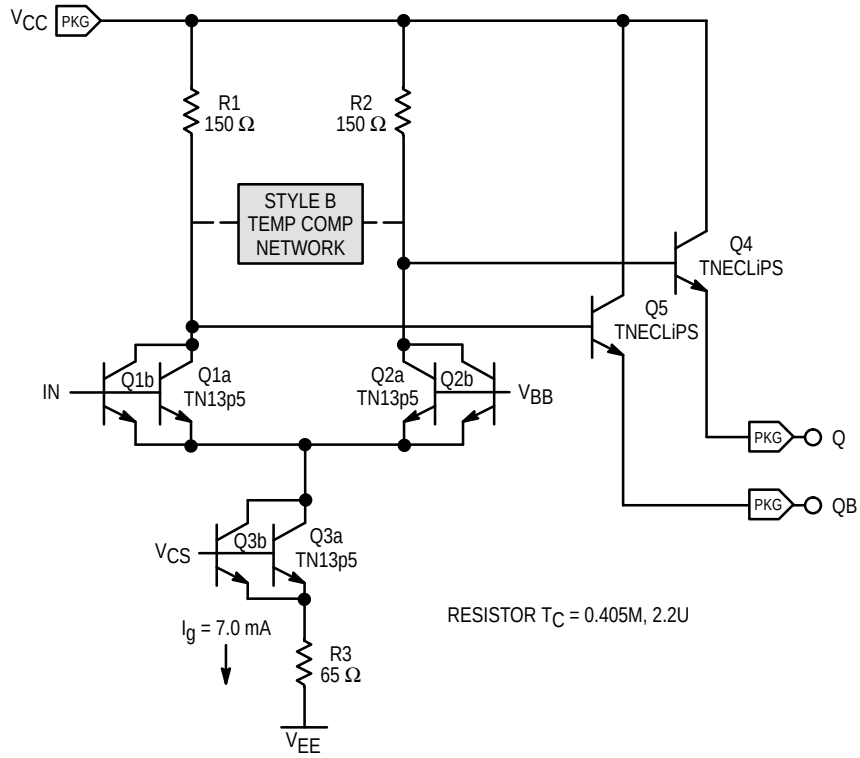

Figure 5. 2x Current Output Schematic

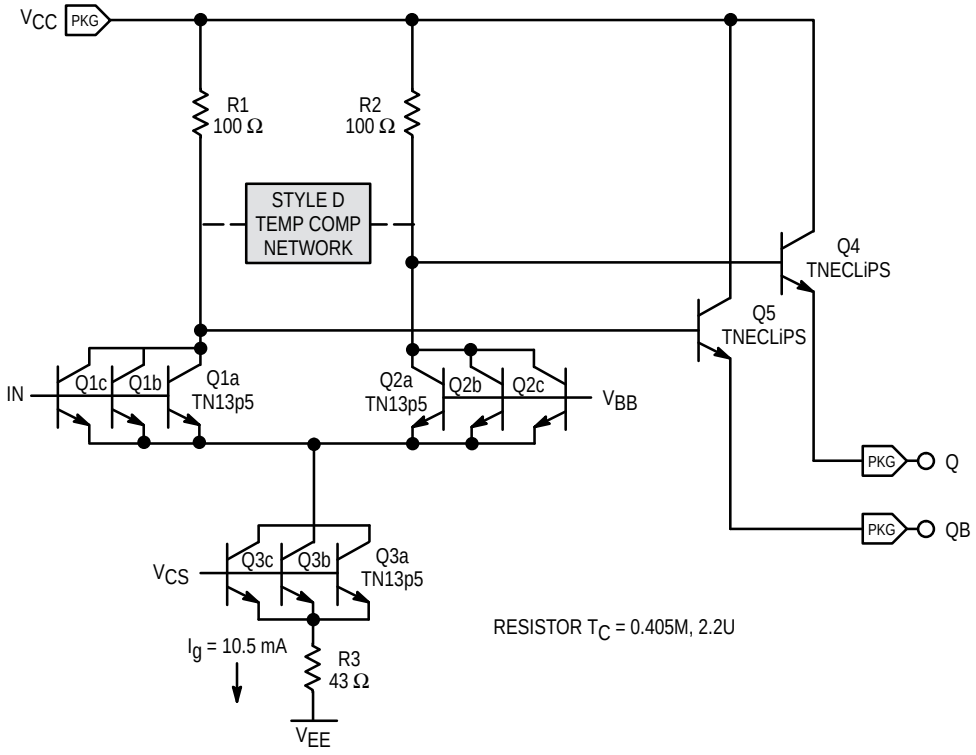

Figure 6. 3x Current Output Schematic

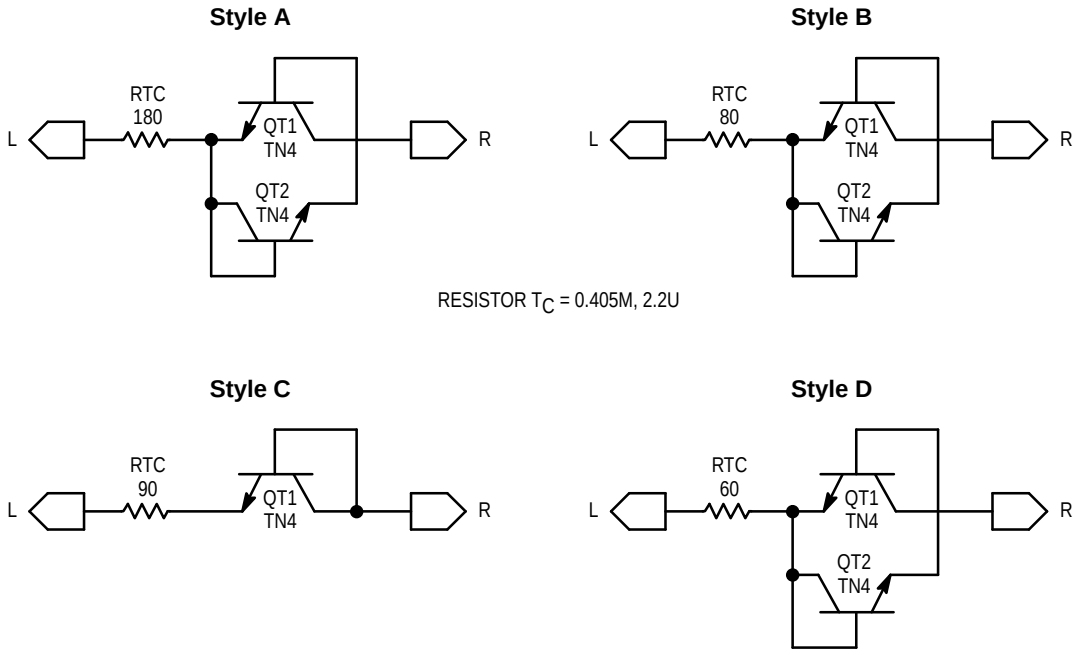

Figure 7. Temperature Compensation Networks

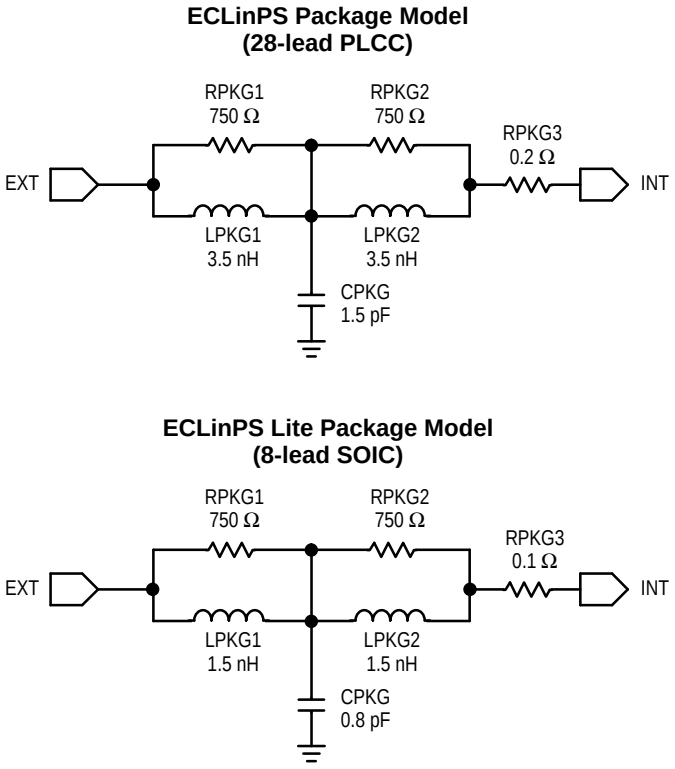

Figure 8. Package Model Schematics

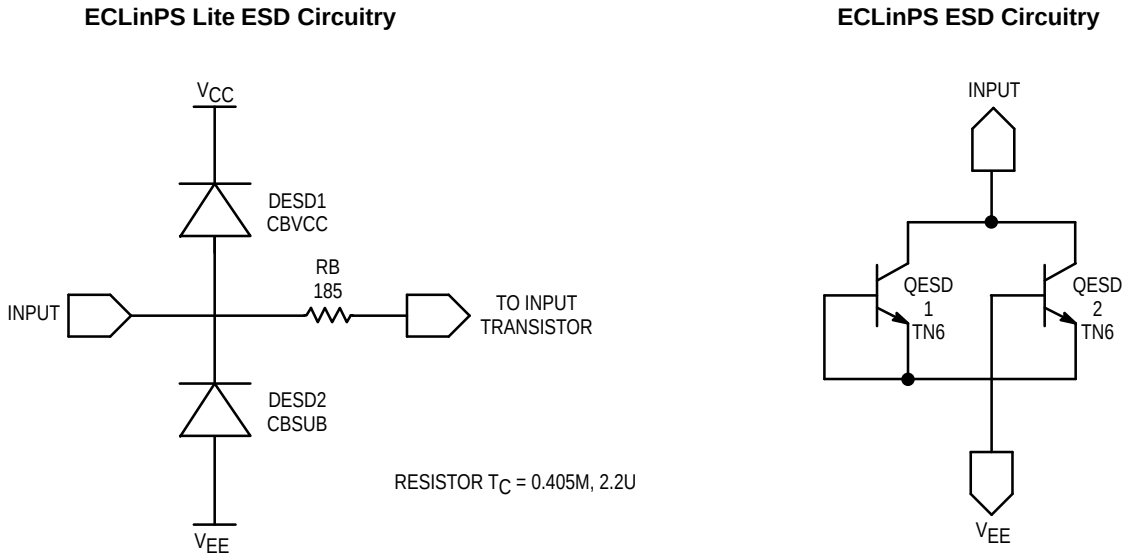

Figure 9. ESD Protection Circuitry

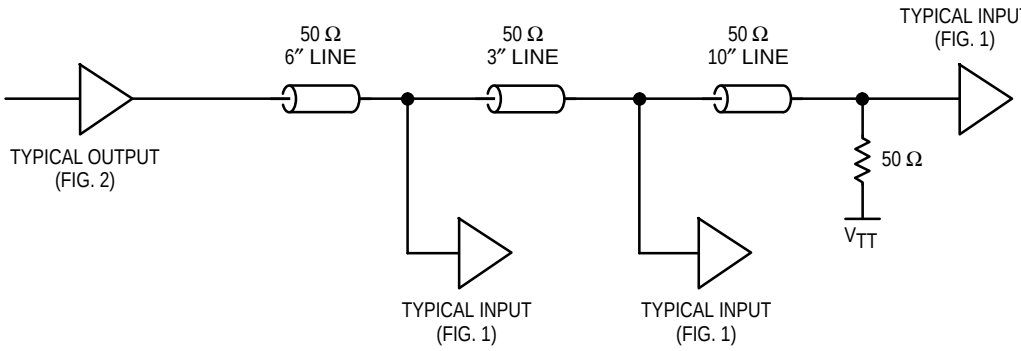

Figure 10. Typical Application for I/O SPICE Modeling Kit

APPENDIX

Schematic/ECLinPS Device Cross Reference

Typical Input	Differential Input	Combination I/O (Gates)
ECLinPS E016, E131, E141, E142, E101, E104, E107, E112, E143, E150 (LEN, MR), E116, E122, E150 (Data), E151, E154, E155, E156, E158 (Data), E158 (SEL), E160, E163, E166, E167, E171, E193, E241, E256, E336, E337	E111, E451, E195, E196, E404, E416, E431, E452, E457, E211	E101, E104, E107, E112, E116, E122, E150 (D), E158 (D), E157 (D)
ECLinPS Lite EL01, EL12, EL31, EL32 (R), EL33 (R), EL35, EL51 (D, R)	EL05, EL11, EL16, EL32 (CLK), EL33 (CLK), EL51 (CLK), EL52, EL89	

Multiple Output Cell	25Ω Bus Outputs	2x Current Output
ECLinPS E112, E212	E336, E337	E195, E196, E211, E404, E457
ECLinPS Lite EL12*		EL01, EL04*, EL05, EL07*, EL11, EL16, EL31, EL32, EL33, EL35, EL51, EL52, EL58*, EL89

3x Current Output	Standard Output
E416	All Others

* These ECLinPS Lite device's inputs feed directly into the output buffer.

SPICE Transistor Model Parameters

```
**** 1.75u x 4.0u emitter
.MODEL TN4          NPN
+ ( IS= 5.27E–18   BF=120   NF=1   VAF=30   IKF=6.48mA
+   ISE= 2.75E–16 BR=10     NE=2   VAR=5     IKR=567uA
+   IRB= 8.1uA      RB= 461.6  RBM= 142.5  RE= 21.6  RC= 83.1
+   CJE= 19.9fF    VJE= .9     MJE= .4             XTB= 0.73
+   CJC= 25.1fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 49.6fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS         TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 17.0mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)*
*

**** 1.75u x 4.75u emitter
.MODEL TN4P75          NPN
+ ( IS= 6.50E–18   BF=120   NF=1   VAF=30   IKF=8.0mA
+   ISE= 3.40E–16 BR=10     NE=2   VAR=5     IKR=700uA
+   IRB= 10uA      RB= 378.5 RBM= 120  RE= 17.5  RC= 74.0
+   CJE= 23.6fF    VJE= .9     MJE= .4             XTB= 0.73
+   CJC= 27.4fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 53.8fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS         TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 21.0mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*
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SPICE Transistor Model Parameters (cont.)

```
**** 1.75u x 6.0u emitter
.MODEL TN6          NPN
+ ( IS= 8.56E–18   BF=120   NF=1   VAF=30   IKF=10.5mA
+   ISE= 4.48E–16 BR=10     NE=2   VAR=5     IKR=922uA
+   IRB= 13.2uA      RB= 291.4  RBM= 95.0  RE= 13.3  RC= 62.7
+   CJE= 29.9fF    VJE= .9     MJE= .4             XTB= 0.73
+   CJC= 31.2fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 60.9fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS         TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 27.6mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*

**** 1.75u x 13.5u emitter
.MODEL TN13P5          NPN
+ ( IS= 2.09E–17   BF=120   NF=1   VAF=30   IKF=25.7mA
+   ISE= 1.09E–15 BR=10     NE=2   VAR=5     IKR=2.25mA
+   IRB= 32.2uA      RB= 122.6  RBM= 42.2  RE= 5.44  RC= 32.8
+   CJE= 67.4fF    VJE= .9     MJE= .4             XTB= 0.73
+   CJC= 53.8fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 103fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS         TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 67.5mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
*

****ECLinPS Lite ESD Diodes
.MODEL CBVCC D
+ (IS= 1.00E–15  CJO= 527fF  Vj= 0.545  M= 0.32  BV= 14.5  IBV= 0.1E–6
+ XTI= 5  TT=1nS)

.MODEL CBSUB D
+ (IS= 1.00E–15  CJO= 453fF  TT= 1nS)


**** Output Emitter Follower
.MODEL TNECLIPS          NPN
+ ( IS= 2.27E–16   BF=120   NF=1   VAF=30   IKF=279mA
+   ISE= 1.19E–14 BR=10     NE=2   VAR=5     IKR=24.4mA
+   IRB= 349uA      RB= 15.98  RBM= 4.17  RE= .501  RC= 11.1
+   CJE= 611fF    VJE= .9     MJE= .4             XTB= 0.73
+   CJC= 440fF    VJC= .67  MJC= .32           XCJC= .3
+   CJS= 668fF    VJS= .6    MJS= .4            FC= .9
+   TF= 8pS         TR= 1nS   XTF= 10    VTF= 1.4V   ITF= 733mA
+   ISC= 0   EG=1.11   XTI= 4.0   PTF=0   KF=0   AF=1   NR=1    NC=2)
```

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