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APPLICATION NOTE

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Driving High Capacitance DRAMs In An ECL System

INTRODUCTION

In present day computer/controller systems where speed and efficiency are of the utmost importance, system designers are using mixed technology in their designs to achieve the necessary speed, power, cost and processing capability desired in high speed data processing systems.

The logic type most applicable to the high speed function of such a system is Emitter Coupled Logic (ECL). Motorola's 10K, 10H, and ECLinPS devices make it possible to operate with clock rates up to 1 GHz. However there are sections of a system where ECL speeds are not necessary. For example, in the area of bulk memory that is not accessed every clock cycle a large CMOS DRAM is less costly, uses less power and takes up less board space per bit than an ECL memory. Now, since ECL and CMOS are of different logic forms and their signal levels are not compatible there needs to be a level translation to enable the two logic families to be used together. The Motorola MC10H/100H660 4-BIT ECL-TTL LOAD REDUCING DRAM DRIVER was designed for this purpose. The H660 is shown in a simplified typical system application in Figure 1.

This paper will explain the features that were designed into the H660 and how to apply them in a mixed technology system to obtain the best performance versus power ratio.

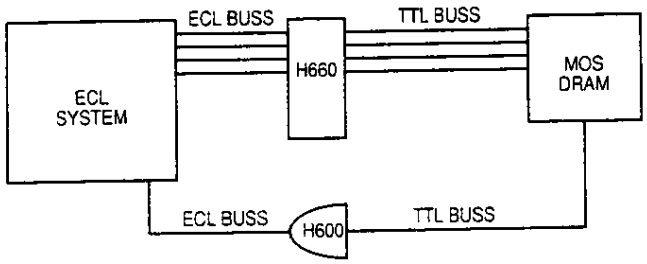
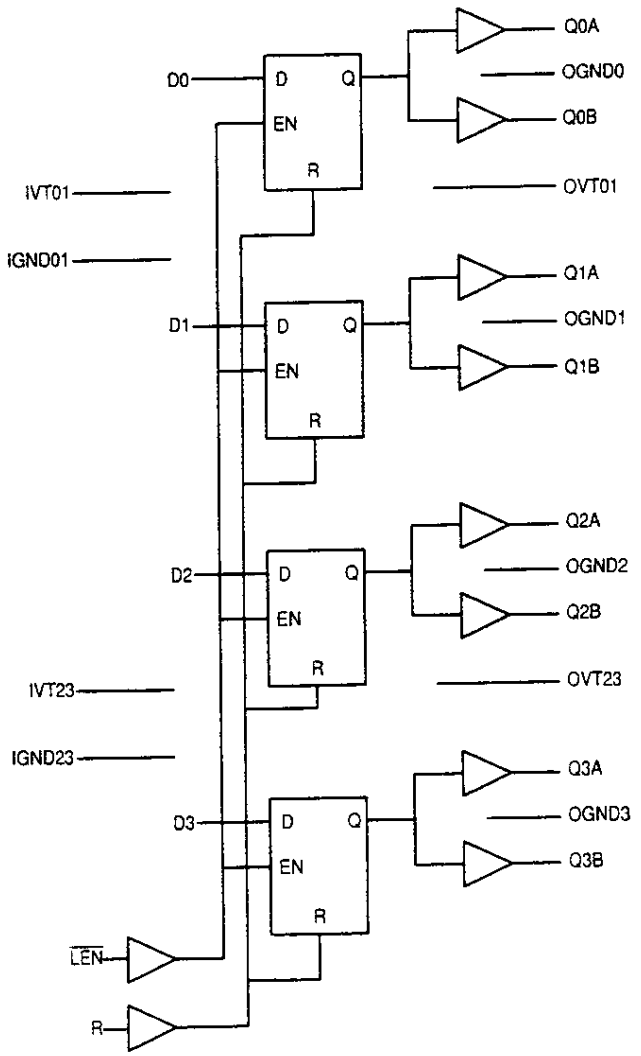


Figure 1.

SYSTEM DESIGN

To switch highly capacitive loads at speeds of a few nanoseconds, the device must supply a large amount of current to charge the lines then it must sink this current to discharge them. This fast switching on an unterminated line can result in a substantial amount of over shoot and ringing.

To eliminate the overshoot and ringing, a small value series resistor (Rs) can be placed at the driver. Figure 4 shows an application of the H660 with a series resistor.



MC10/100H660 Logic Diagram

FEATURES OF THE H660 DRAM DRIVER

The H660 translates the ECL signal to a TTL level suitable for driving DRAM memories with high input capacitance.

The input impedance of the 660 varies with frequency, at 10 MHz it is typically about 150 to 250 ohms and goes down to about 50 to 60 ohms at 200 MHz as shown in Figure 2.