APPLICATION NOTE

AN109
Microprocessor-compatible DACs

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Philips
Semiconductors

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DAC products are designed to convert a digital code to an analog signal. Since a common source of digital signals is the data bus of a microprocessor, DAC circuits that are bus compatible ease the design engineer's interface problems.

WHAT FEATURES MAKE A DEVICE BUS-COMPATIBLE?

The five conditions which determine processor bus compatibility are:

- Inputs must present low bus load
- Addressing must be provided
- Inputs must be latched
- Logic thresholds must be compatible
- Timing requirements should be adequate (<1µs)

Philips Semiconductors' microprocessor-compatible DACs, the NE5018 series, meet these requirements. In addition, they provide an internal reference source. The NE5018 provides a scaled voltage output, eliminating the need for an external op amp. The NE5118 is identical to the NE5018, except it provides the user with a current output. Figure 1 shows a typical microprocessor system with analog output using the NE5018 to provide a programmable voltage and an NE5118 to provide a programmable current.

The following discussions detail the operation of the NE5018 and NE5118 series DACs.

LATCH CIRCUIT

The latch circuits of the NE5018 and NE5118 are identical. Both the data inputs and latch enable ($\overline{LE}$) input feature ultra-low loading for ease of interfacing. The 8-bit data latch, controlled by the latch enable input, is static and level sensitive. When ($\overline{LE}$) is low, all the latches become transparent and the output changes as the bit pattern changes on the data bus. When the latch enable returns to its high state, the last set of inputs are held by the latch and a unique output corresponding to the binary word in the latch is produced. While the latch enable is high, the latch inputs represent a high impedance load on the data bus and changes on the data bus have no effect on the DAC output.

The digital logic input for the NE5018 and NE5118 series DACs utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). To be compatible with microprocessors, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor and I/O data bus lines. Figure 2 gives the typical timing requirements of the latch circuits in the NE5018 and NE5118.

The voltage levels on the data bus should be stable for approximately 150ns before latch enable returns to high level. The timing diagram shows 100ns is required for setup time and the information on the data lines should remain valid for another 50ns.

REFERENCE INTERFACE

The NE5018 and NE5118 contain an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 12) allows easy trimming of the reference output (Pin 13). Use of a 10k pot and series resistor, as shown in Figure 3, adjusts the gain of the buffer amplifier, therefore varying the output reference voltage level.

This network can then be used as a full-scale output adjust. A variation in the $V_{REF\ OUT}$ of ~ 0.8V, results in a corresponding 1.6V variation in the full-scale output. This is more than adequate since the untrimmed $V_{REF\ OUT}$ is typically within 200mV of the nominal 5V. The $V_{REF\ OUT}$ will provide a maximum of 5mA drive and can be used as a reference voltage for other system components, if required.

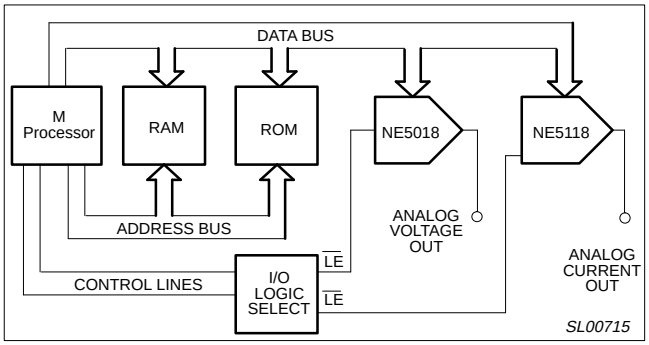

Figure 1. Interfacing to a Microprocessor

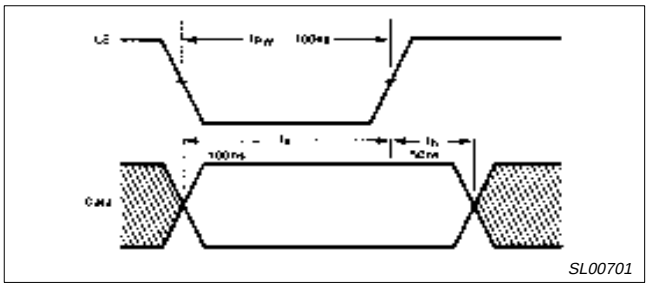

Figure 2. Latch Enable ($\overline{LE}$) Timing Diagram for the NE5018 and NE5118

Since a potential need exists to use the NE5018 and NE5118 as multiplying DACs, the V_{REF} is not connected internally, allowing the use of external reference sources. To utilize the internal reference, the $V_{REF\ OUT}$ (Pin 13) must be jumper-connected to the $V_{REF\ IN}$ (Pin 14). This also makes it possible to use a common reference for other D/A or A/D circuits in a system.

INPUT AMPLIFIER OF THE NE5018

The DAC reference amplifier has been designed to eliminate the need for compensation when operating from the internal reference or from an external reference which is buffered by an op amp or low impedance source. Compensation is required, however, when operating from a high impedance source. The addition of an external resistance reduces the phase margin of the amplifier making it less stable. Compensation, when required, is a single capacitor from Pin 16 to ground.

Figure 4 details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5V V_{REF}. This current sets the

input bias to the ladder network. Data bit 7 (DB_7) Q_7, when turned on, will mirror this current and will contribute 1mA to the output. DB_6 (Q_6) will contribute of that value or 0.5mA, and so on. If all bits are on, the output current will be

2mA-1 LSB. The full-scale V_{OUT} will be ($I_{OUT}R_F$) or 2mA-1 LSB×5k)=(10V-1 LSB)=9.961V. The overall input/output expression for the NE5018 is:

$$V_{OUT} = 2V_{REF} \times \left(\frac{DB7}{2} + \frac{DB6}{4} + \frac{DB5}{8} + \frac{DB4}{16} + \frac{DB3}{32} + \frac{DB2}{64} + \frac{DB1}{128} + \frac{DB0}{256}\right)$$

The minimum current for the ladder network to be operative in the linear region is 500µA. Therefore, the minimum V_{REF} input is 2.5V. The slew rate of the reference amplifier is typically 0.7V/µs without compensation. The input structure of the NE5118 is slightly different and will be discussed in greater detail later. Q_T provides a termination for the R-2R ladder network and does not contribute to I_{OUT}.

OUTPUT INTERFACE OF THE NE5018

The NE5018 has an internal op amp which provides a voltage output, while the NE5118 is a current output device. The NE5018 output op amp is a two-stage design with feed-forward compensation. Having a slew rate of 10V/µs, it provides a voltage output from 0 to 10V (±0.2%) typically within 2µs (the time allowed for the output voltage to settle to within LSB). Compensation must be provided externally as shown in Figure 5.

The addition of the optional diode between the summing node (Pin 20) and ground prevents the DAC current switches from driving the op amp into saturation during large-signal transitions which would increase the settling time.

Zero adjust circuits, such as the one shown in Figure 5, may also be connected to the summing node to provide a means to zero the output when all zeros are present on the input. Not all applications require a zero adjust circuit since the untrimmed zero-scale is typically less than 5mV. Excess stray capacitance at the sum node of the output op amp may necessitate the use of a feedback capacitor from V_{OUT} to the sum node (C_{FF}) to insure stability of the op amp. Typical values of C_{FF} range from 15 to 22pF. The rated load of the op amp is ~ 2kΩ. For stability, the load capacitance should be minimized (50pF max).

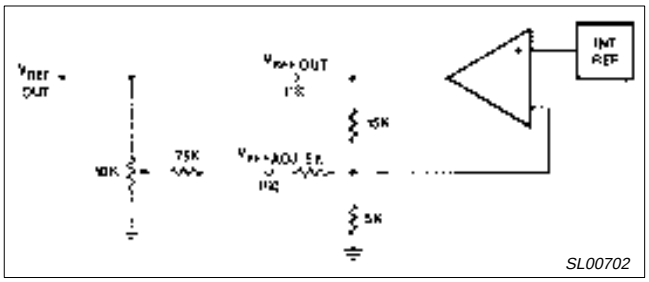

Figure 3. Reference Adjust Circuit

MODES OF OPERATION OF THE NE5018

The NE5018 has two basic modes of operation: unipolar and bipolar. When operating in the unipolar mode, the output range is 0 to +10V. To change from unipolar to bipolar operation, the bipolar offset pin is connected to the summing node. This provides the 5V offset required for this mode of operation. The output now will have a range from -5 to +5V. Figure 6 details the connection of the NE5018 in the bipolar mode of operation.

With the bipolar offset, Pin 15, connected to the sum node, Pin 20, it forms a unity gain inverter with an input of $+V_{REF}$. The bipolar offset develops an I_{REF} current through the internal 5k resistor. This current is then fed to the sum node of the output amplifier where it is summed with the current output of the DAC ladder network. Assume for the moment that the current output of the ladder network is 0mA. With a V_{REF} equal to +5V, I_{REF} is 1mA and the output of the op amp is converted to -5V. If the DAC switches are now set to full-scale, the current from the DAC ladder is 2mA. This is summed against the 1mA I_{REF} and causes the output of the op amp to swing from -5V to +5V.

$(I_{DAC}-I_{REF})5k=(2mA-1mA)5k=+5V$

Since the bipolar offset resistor is monolithic, tracking with the 5k feedback resistor of the output amplifier is excellent.

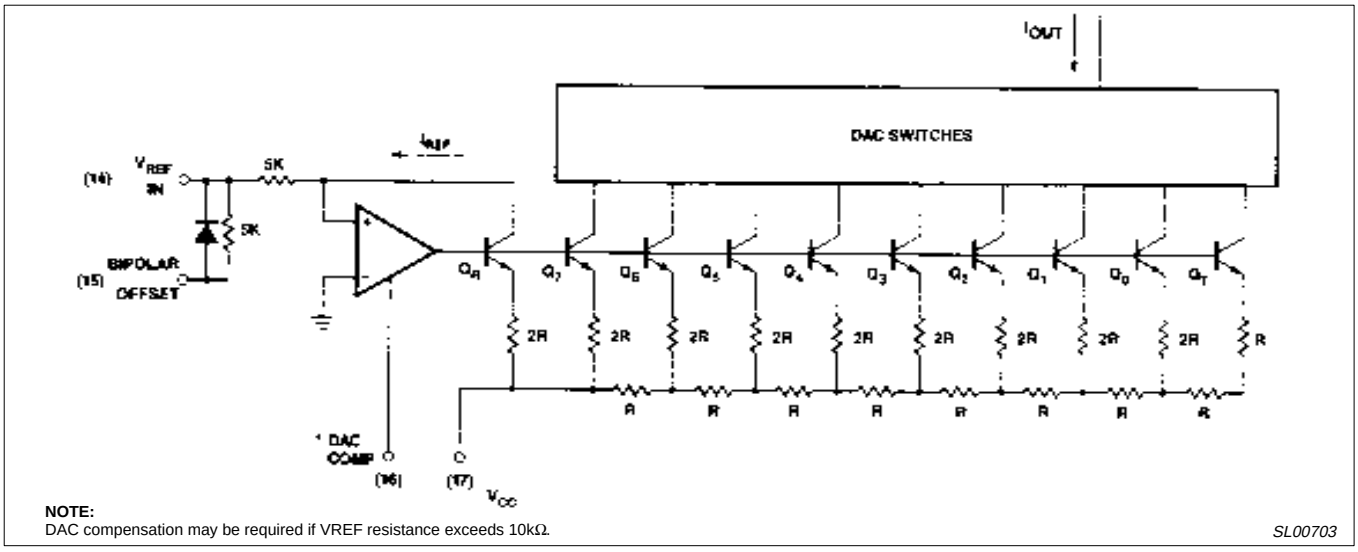

Figure 4. R-2R Ladder Network Develops a Scaled Reference Current Value Into the DAC Switching Network

Note that the bipolar offset pin could not be used when using the DAC in a multiplier application since the V_{OUT} would reflect an inverted input signal.

NOTES ON THE NE5118 CURRENT OUTPUT DAC

The basic operation of the NE5118 current output DAC is the same as the NE5018. The current output structure allows the user to provide a programmable current sink (I_{OUT} max of 2mA). Several jumper options provide a variety of operational modes. Figure 7 is a block diagram of the NE5118. The input logic and V_{REF} portions are identical to the NE5018.

REFERENCE INPUT AMPLIFIER

The characteristics of the reference input amplifier are identical to the NE5018; however, extended versatility of the input structure allows for both current (via Pin 14) or voltage (via Pin 15) reference inputs.

The maximum DAC output current is 2mA. The DAC has an internal gain of 2, limiting the maximum usable input current to 1mA.

NOTE:
The absolute maximum input current should be limited to 5mA to prevent damage to the input reference amplifier.

Figure 8 shows the basic operating mode of the NE5118 using an external current reference resistor (R_1) and a positive reference voltage.

This voltage can be provided by either an internal or external reference voltage. Figure 9 shows a typical connection using a voltage input directly via Pin 15.

Besides a reduced parts count, use of the internal R_{REF} provides excellent tracking characteristics with the R_{OUT} resistor (Pin 20) when developing a high slew rate voltage output. The negative V_{REF} input must be returned to ground directly or through R_2. R_2 is optional and is used to cancel minor errors developed by the input bias currents of the reference amplifier ($R_2=R_1$ in Figure 8). A negative voltage can be the reference by using the $-V_{REF}$ input pin as shown in Figure 10.

The positive V_{REF} is returned to ground via R_{IN} (Pin 15). As with the NE5018, a compensation capacitor on Pin 16 is not required if the V_{REF} is supplied by a low impedance source.

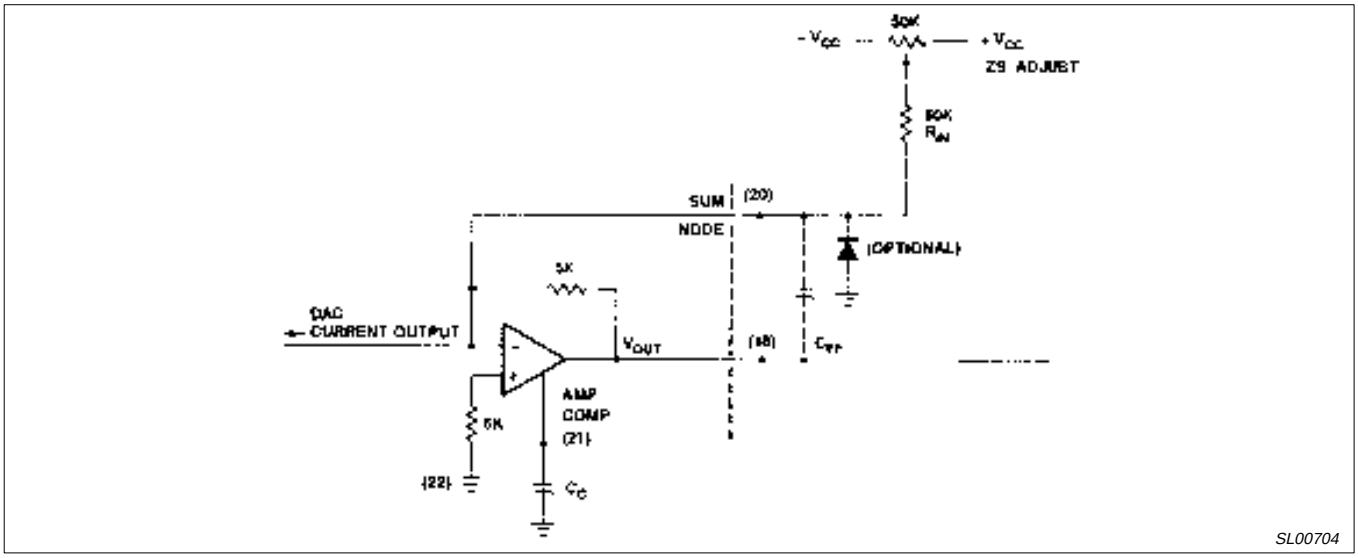

Figure 5. Zero-Scale Adjust

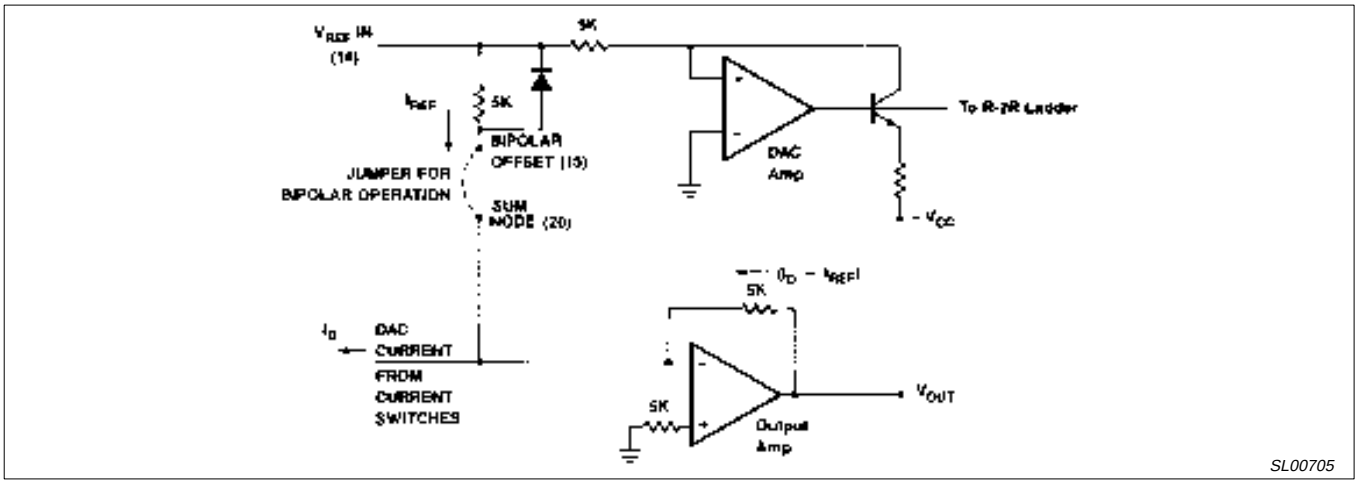

Figure 6. Bipolar Output

OUTPUT STRUCTURE

The output of the NE5118 is a current sink with a capacity of 2mA (full-scale) capable of settling to 0.2% in 200ns. Internal bias and feedback resistors are also made available to ease the designer's task of interfacing.

Figure 11 shows the NE5118 using a current-to-voltage converter at the output to provide a high slew rate voltage output. Using the NE538 as shown can provide 60V/µs slew rate output. The diode at the inverting node of the op amp improves the response time by preventing saturation of the op amp during large signal transitions. The feedback resistor R_{OUT1} (Pin 20) is provided internally,

providing excellent thermal tracking characteristics with the R_{REF} at the input.

Bipolar operation can be accomplished by connecting the $V_{REF\ OUT}$ (Pin 12) to the R_{OUT} resistor (Pin 20) (Figure 12). The principal is the same as the NE5018 bipolar operation. The internal resistors exhibit excellent thermal tracking characteristics.

An alternate method of bipolar output operation is shown in Figure 12. The R_{REF} and R_{OUT} set up a current-to-voltage converter while two (2) external resistors provide a bipolar offset. R_{EXT1} and R_{EXT2} should have similar thermal tracking characteristics.

The NE5118 can provide a voltage output directly when driving a high impedance load as shown in Figure 13. With a full-scale current of 2mA, Pin 20 tied to +10V and a digital input of zero, the high impedance load will see +10V. For a full-scale digital input, the load will see 0V. Since the load and the internal resistor form a voltage divider, their ratio determines full-scale accuracy.

By connecting the R_{OUT} resistor (Pin 20) to ground (Figure 13), the output voltage seen by the load ranges from 0V as zero-scale to -10V as full-scale. Only a few of the many possible output configurations have been shown to demonstrate the NE5118 flexibility.

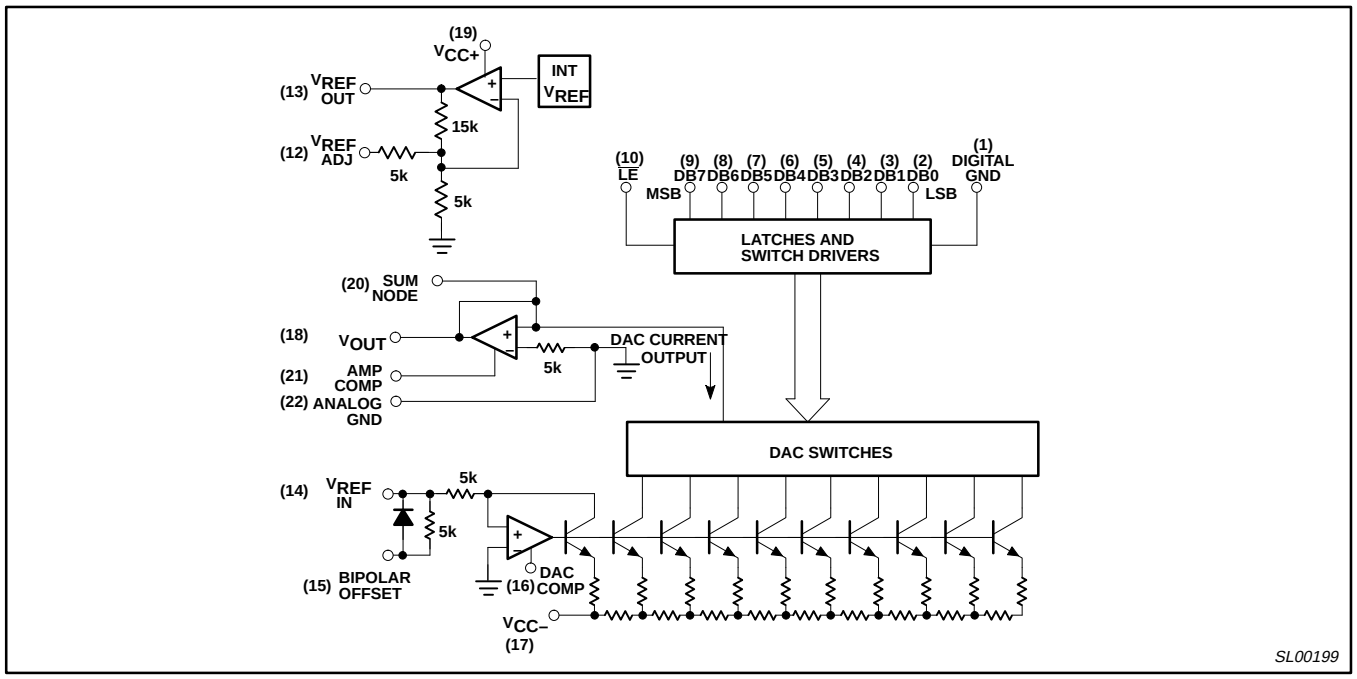

Figure 7. Block Diagram

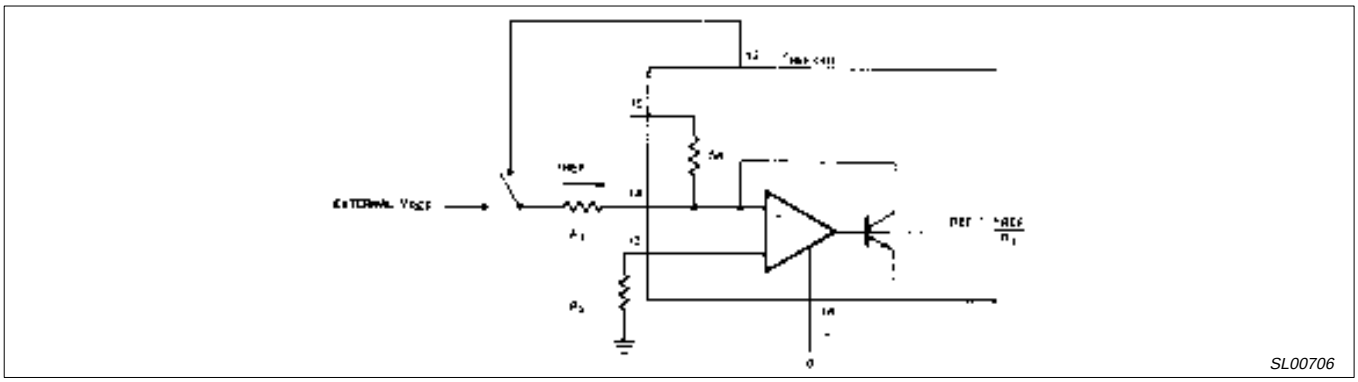

Figure 8. Positive I_{REF}

CIRCUIT EXAMPLES

Now that the basics of the NE5018 and the NE5118 have been discussed, let's examine some specific circuits. Figure 14 is a microprocessor-controlled programmable gain amplifier, using the NE5018. The V_{REF} output is fed to the non-inverting input to a differential amplifier. R_1+R_2 places 2.5V_{DC} bias on the V_{REF} input. R_2 can be made adjustable to precisely control the DC reference input. The analog input is fed to the inverting input of the differential amplifier with a gain of unity. An input range of 0 to 2.5V will produce an output of 10V to 5V full-scale. $V_{REF\ IN}$ will vary from 5V to 2.5V. The current ladder is always kept in the linear operating range and the output will not become distorted.

No compensation is required for the DAC reference amplifier since the $V_{REF\ IN}$ is fed from a low impedance source. With a compensation cap of 33pF on the output amplifier, the frequency response of the output is linear to at least 20kHz with less than 0.1% distortion with an input amplitude of 1V_{P-P}. The NE5018 is seen by the microprocessor as an I/O device.

In Figure 15, the N5018 and NE5118 provide a method of summing two digital words and generating a voltage output. The latch enable feature of both devices direct connection to a data bus, using address decoding. These devices greatly reduced the total component count required to perform this operation.

The reference voltage is common to both DACs, being provided by the NE5018. The bipolar offset resistor of the NE5018 provides the 1mA current reference for the NE5118. Using the internal resistor of the NE5018 to develop the reference current enhances the thermal tracking since the current-to-voltage resistor of the output op amp is also in the NE5018. Both DACs can be addressed by a microprocessor using an address decoder to select DAC A or DAC B.

Figure 16 is a schematic of the NE5118 and a NE527 as a high-speed programmable limit sensor (or A/D converter). A 4.8V zener diode is used on the comparator input to insure the input voltage range of the comparator is not exceeded. The outputs of the NE527 comparator are complementary, easing the logic interface requirement. If the strobe function is not used, the strobe inputs should be tied high, through a 10kΩ resistor.

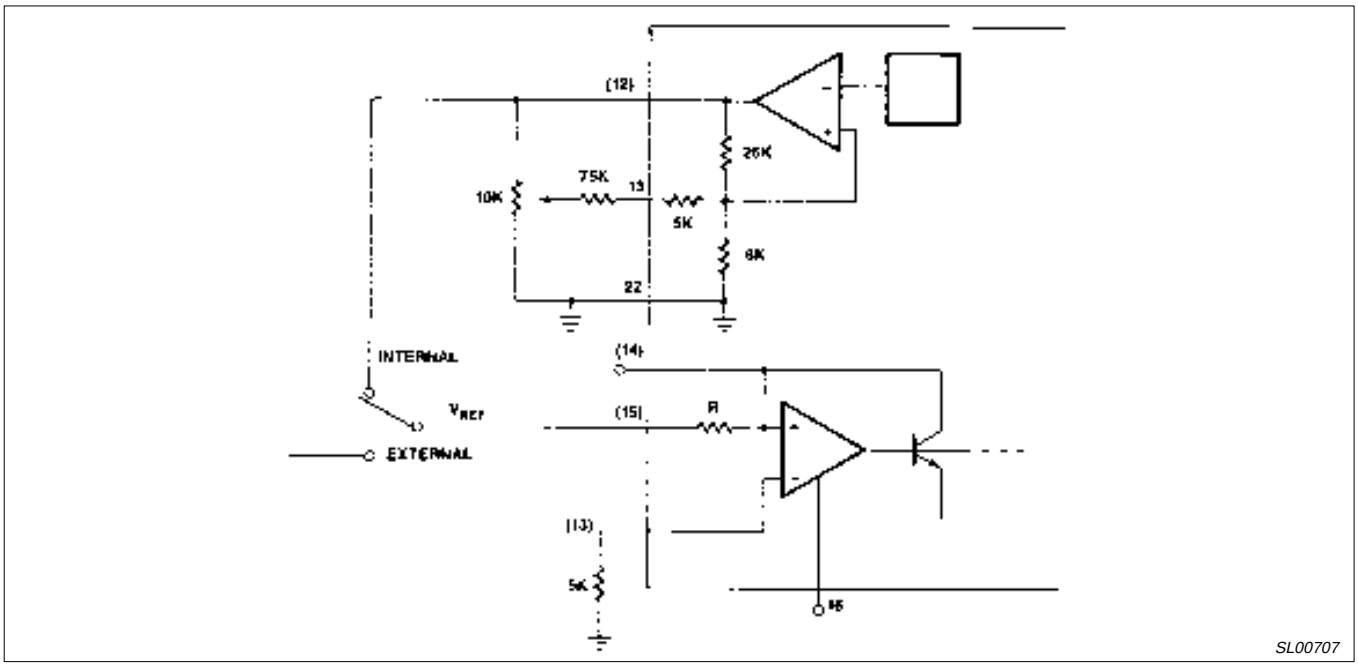

Figure 9. Positive V_{REF}

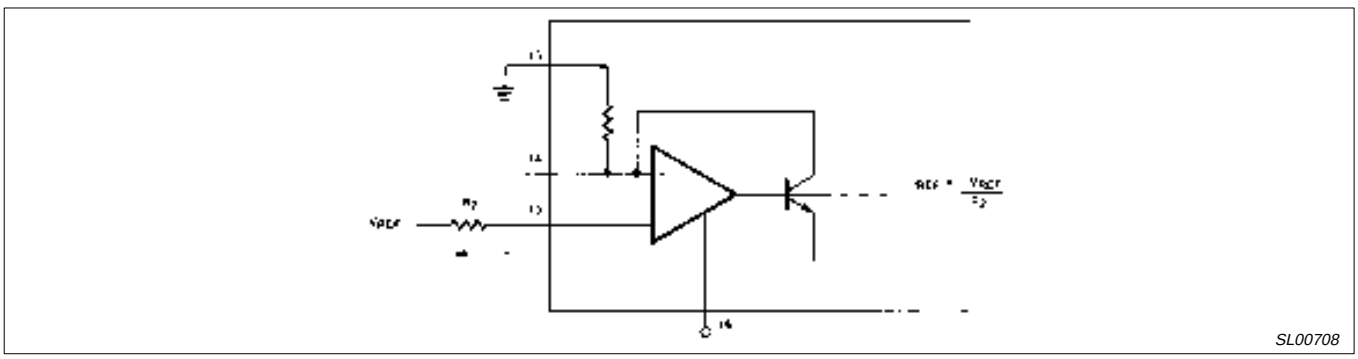

Figure 10. Using a Negative I_{REF}

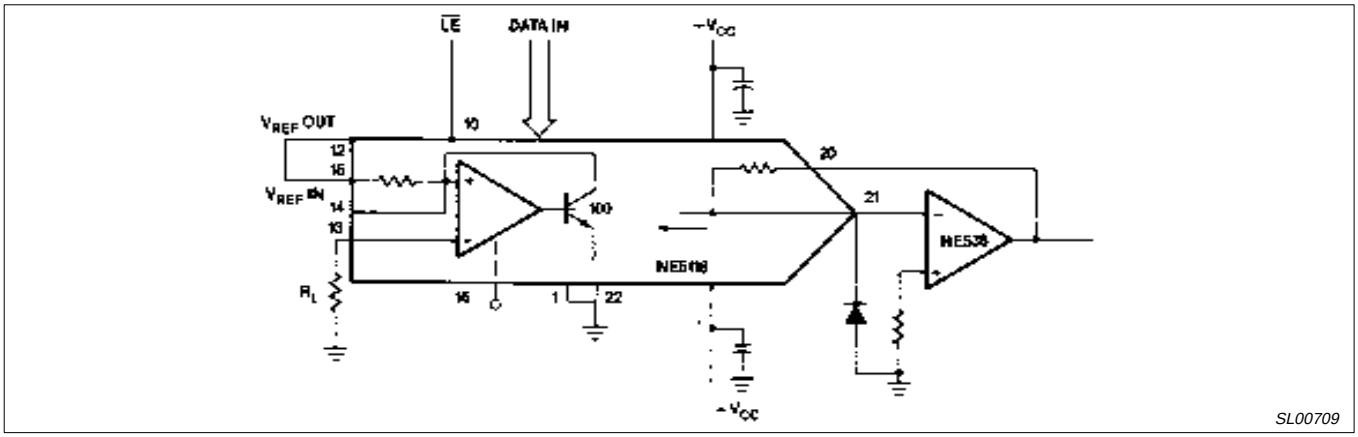

Figure 11. High Slew Rate Voltage Outputs

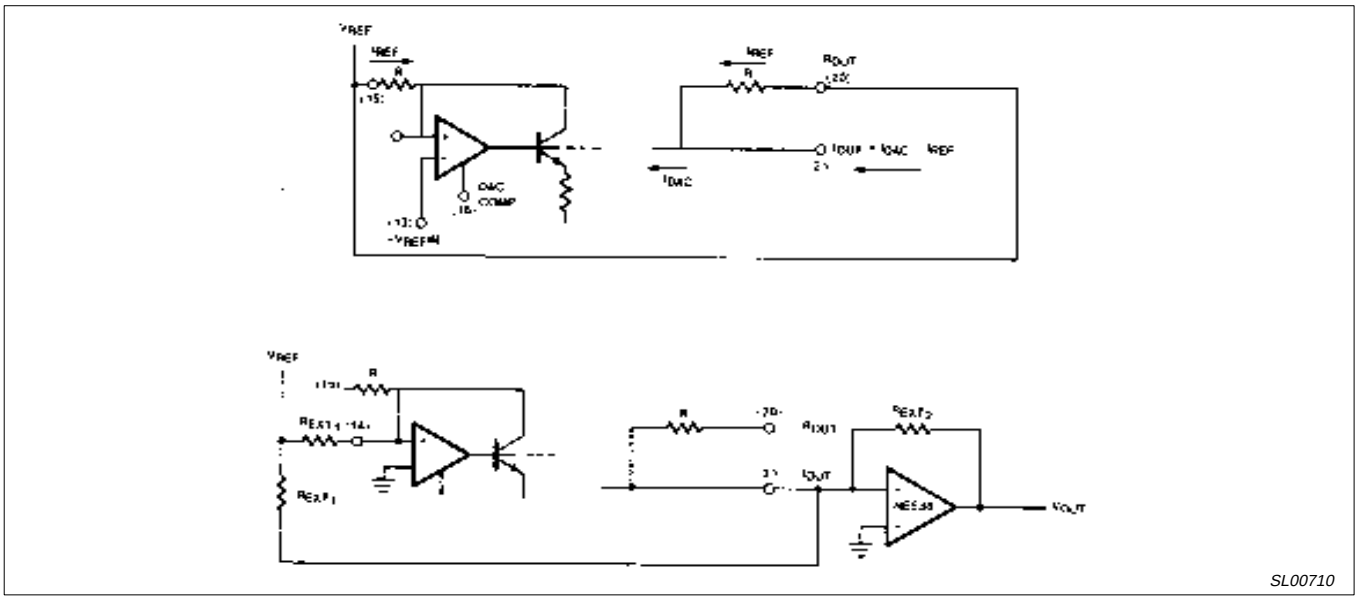

Figure 12. Bipolar Options of the NE5118

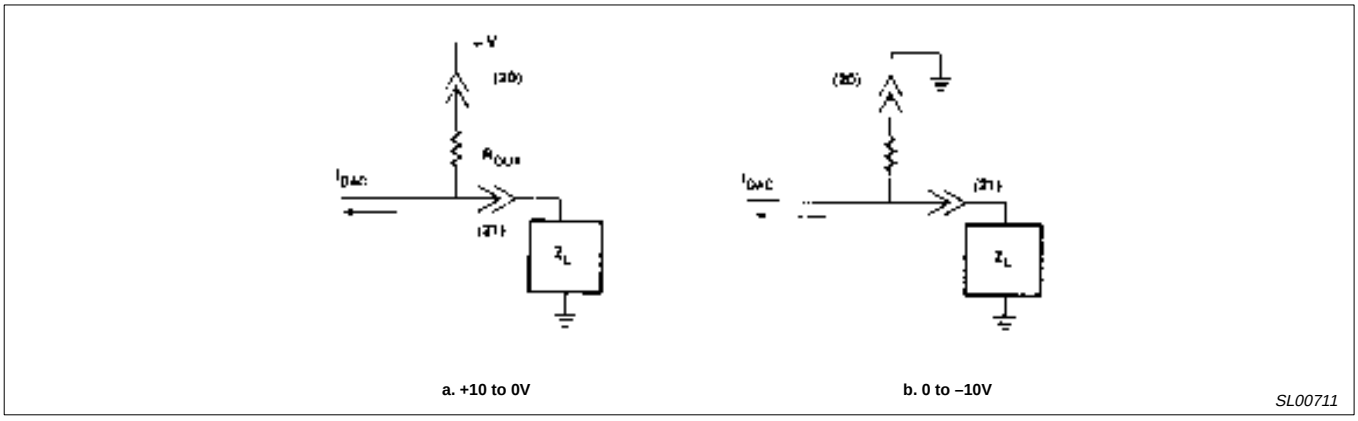

Figure 13.

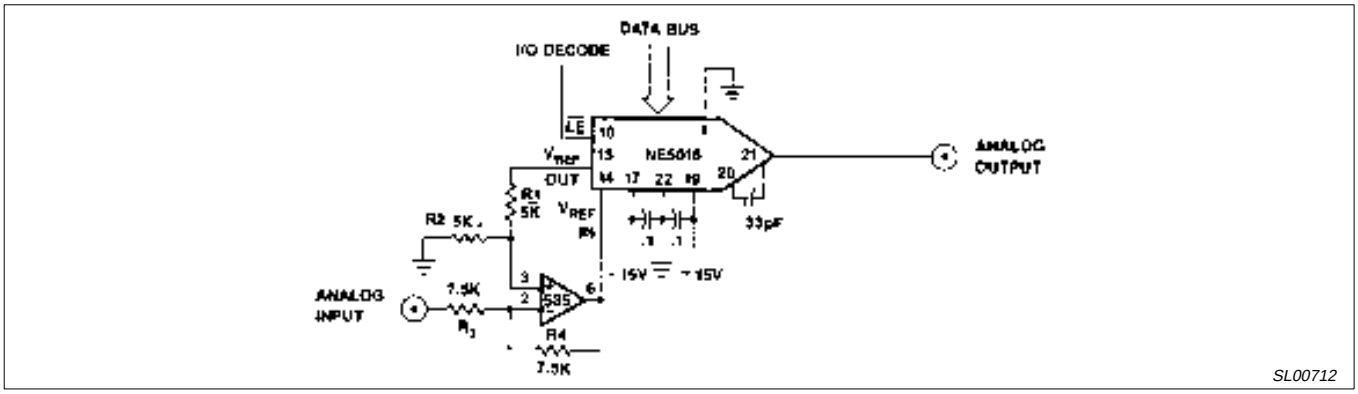

Figure 14. Programmable Gain Amplifier

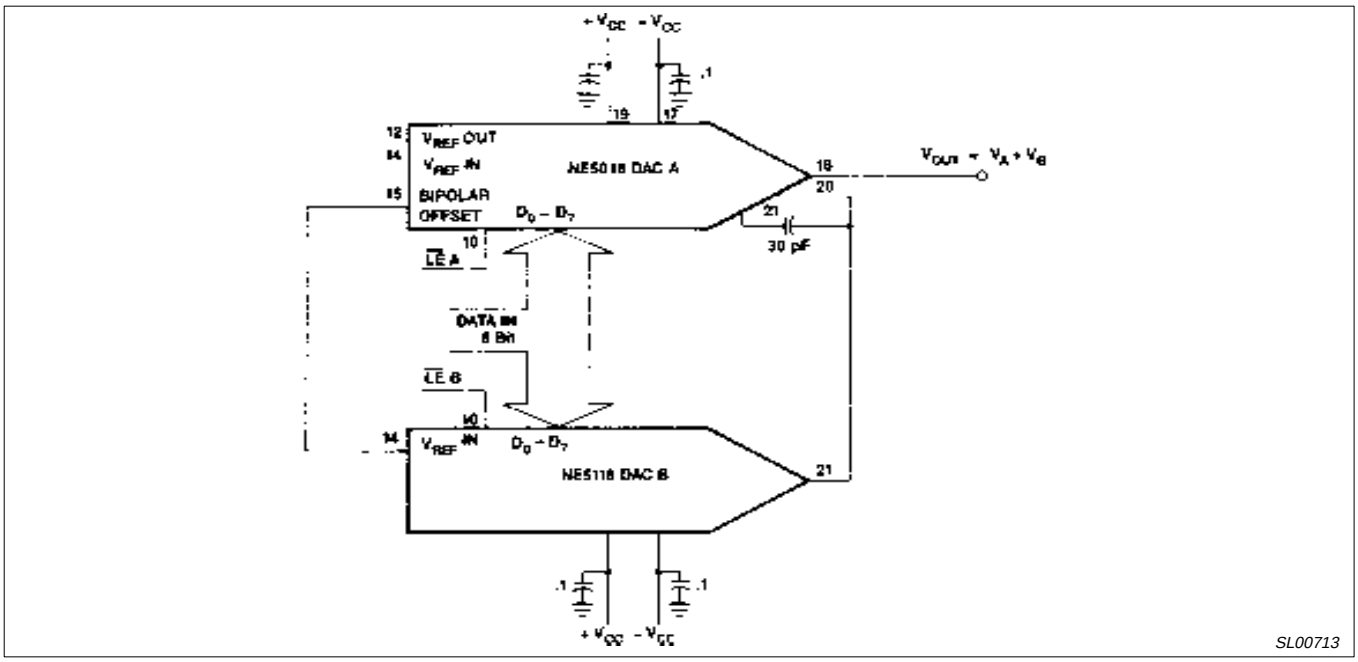

Figure 15. Analog Summation With Digital Inputs

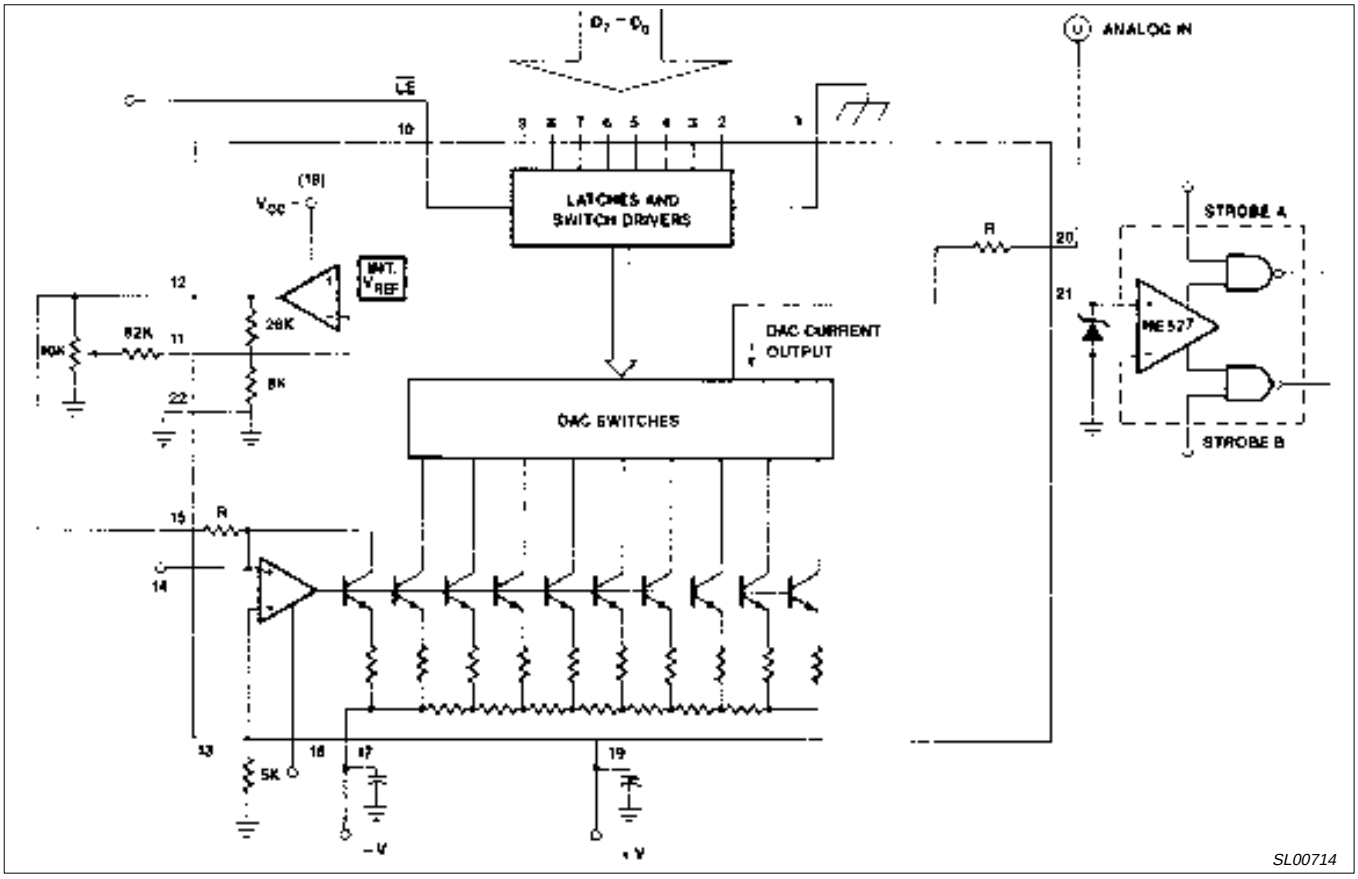

Figure 16. Programmable Limit Comparator