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Adding Digital Volume Control To Speakerphone Circuits

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INTRODUCTION

The volume control provided on many speakerphones is a potentiometer, some rotary and some linear, wired so the wiper provides a varying DC voltage to a variable gain stage. This application note will describe how to replace the potentiometer with a digital circuit which allows control of the speaker volume from a set of "UP" and "DOWN" pushbutton switches. The circuit uses only 3 standard CMOS ICs.

THE MC34018 AND MC34118

The volume control pins (VLC) on the MC34018 and MC34118 speakerphone ICs (Pins 24 and 13 respectively) are similar in they have a very high input impedance (>10 MΩ) and low bias current (+0.2 μA for the MC34018, −60 nA for the MC34118). Additionally, they both function similarly in that the volume control operation is based on the *ratio* of the voltage at VLC to the internally generated reference voltage (V_B shown in Figure 1). The ratio is 1.0 (VLC = V_B) for maximum volume, and less than 1 for reduced volume. The minimum recommended setting is 0.55 V_B for the MC34018, and 0.3 V_B for the MC34118.

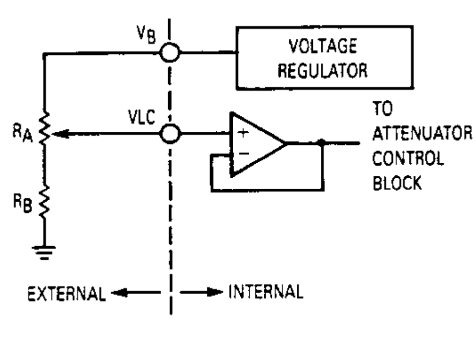

Figure 1. Analog Volume Control Interface

To achieve the same voltage range at VLC with a digital circuit, a binarily weighted resistor network is employed (see Figure 2).

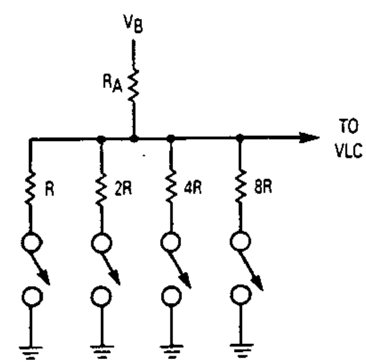

Figure 2. Digital Volume Control Resistor Network

With all switches open, VLC equals V_B (maximum volume). The minimum setting occurs when all switches are closed, and the R_B in Figure 1 is represented by the parallel combination of the four lower resistors (0.533R). The exact value of the resistors will be determined later.

USING UP/DOWN SWITCHES

Controlling the resistor network of Figure 2 is done with the circuit of Figure 3. The four switches of Figure 2 are replaced with the four outputs of the MC14516 Up/Down binary counter and 1N914 diodes. Each of the resistors is "on" when the corresponding output is low, and disconnected (by means of the diode) when the output is high, providing 16 volume levels for the speakerphone. The circuit may be used in a line-powered speakerphone, or one which is powered from a power supply.

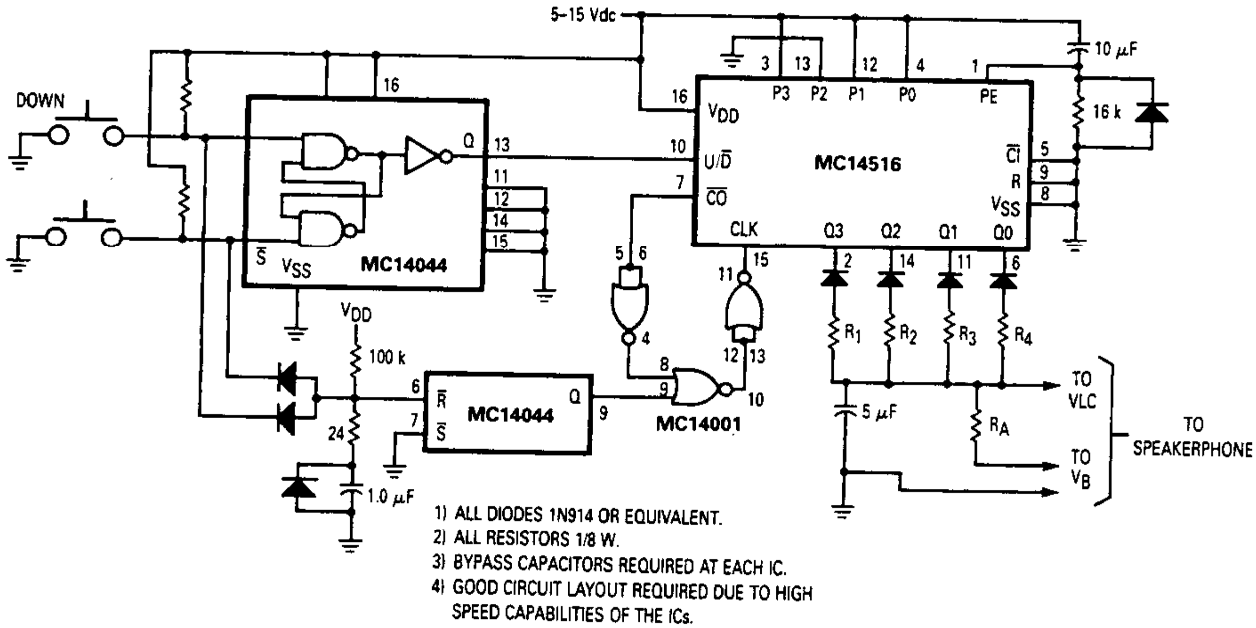

Figure 3. Up/Down Free Standing Digital Volume Control

The circuit works as follows:

- When one of the switches is closed, pin 13 of the MC14044 RS flip-flop is set either high (for UP) or low (for DOWN), and this sets the U/$\overline{D}$ input of the counter.
- Upon closing the switch, the 1.0 μF capacitor is discharged (the 24 Ω resistor limits the current during discharge), and pin 9 of the MC14044, and the counter's CLK input are taken low (assuming the $\overline{CO}$ output of the counter is high).
- Upon releasing the closed switch, the 1.0 μF capacitor will charge up slowly, and the CLK input of the counter will switch high approximately 80 milliseconds later, incrementing or decrementing the counter. The time delay provides for switch de-bounce.
- When maximum count is reached while up-counting, the $\overline{CO}$ output (Pin 7) switches low, preventing any more clock pulses from reaching the counter. The $\overline{CO}$ output returns to high when the U/$\overline{D}$ input changes state (by pressing the DOWN switch), allowing the counter to count down. A similar sequence occurs when minimum count is reached while down-counting.
- The Preset Enable (PE) input receives an active high pulse during power up, thus presetting the outputs to 1011 (in this example). In this way the speakerphone's volume is set to a known state each time the phone is taken off-hook. The preset level may be any of the 16 states by appropriately wiring P3–P0.

As the counter is sequenced up or down, the voltage at VLC will vary between a maximum of V_B and a minimum determined by the resistors (R_A, R_1–R_4). The 5.0 μF capacitor at VLC smooths the transition to the new level, preventing clicks or pops from being heard in the speaker. The power supply voltage can be obtained from the V_{CC} pin of the MC34118 (Pin 4), or from the V_{CC} output pin of the MC34018 (Pin 20). The circuit of Figure 3 requires less than 1.0 μA of supply current when idle, and typically less than 200 μA during a transition.

CALCULATING THE RESISTOR NETWORK

The resistor network values will be calculated for each of the three following situations:

1) The MC34018 speakerphone circuit, which has a fixed V_B of 2.9 Volts, and requires a minimum VLC of 0.55 V_B (1.59 Volts).
2) The MC34118 speakerphone circuit with a **fixed** supply voltage, resulting in a fixed V_B equal to ≈ (V_{CC} − 0.7)/2, and requiring a minimum VLC of 0.3 V_B.
3) The MC34118 speakerphone circuit with a **variable** supply voltage (such as in a line powered phone), resulting in a V_B voltage which can range from 1.3 to 2.8 V, and requiring a minimum VLC of 0.3 V_B.

The reason for the differentiation between #2 and #3 above is due to the voltage drop of the 1N914 diodes (≈0.5 V), which is a significant part of V_B. The voltage drop of the counter's outputs, when a logic "0," is typically <10 mV, and is considered negligible. The resistor network for situations 1 and 2 is shown in Figure 4. Situation 3 will require a slightly different circuit.

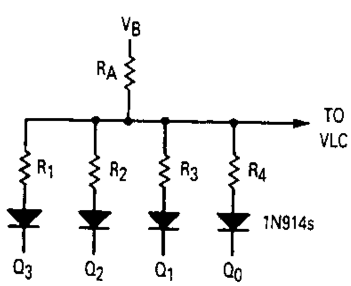

Figure 4. Network for Constant Voltage V_B Circuits

Situation 1

For the MC34018, R_A is selected to be 20 kΩ, as that is the same as the potentiometer's value shown in its data sheet. The voltage at VLC is equals:

$$VLC = \frac{(V_B - 0.5) \times R_B}{20\,k + R_B} + 0.5\,V$$

where R_B is the parallel combination of the "on" resistors. To achieve a minimum VLC of 0.55 V_B, R_B calculates to be 16.8 kΩ. The "R" value for Figure 2 is then 16.8 k/0.533, or 31.5 kΩ. The next lower standard resistor value of 30 kΩ is then chosen for "R," which is R_1 in Figures 3 and 4. Using standard values for the other resistors yields R_2 = 62 kΩ, R_3 = 120 kΩ, and R_4 = 240 kΩ. The resulting performance of this network is shown in the following tabulation:

Q_3–Q_0	"On" Resistors	VLC	VLC/V_B	Δ	dB Gain	Comments
0	R_1 R_2 R_3 R_4	1.57	0.542		−25.5	Min
1	R_1 R_2 R_3	1.61	0.556	0.014	−24.6	Volume
2	R_1 R_2 R_4	1.66	0.571	0.015	−23.5	
3	R_1 R_2	1.71	0.588	0.017	−22.4	
4	R_1 R_3 R_4	1.75	0.604	0.016	−21.3	
5	R_1 R_3	1.81	0.624	0.020	−19.9	
6	R_1 R_4	1.87	0.645	0.021	−18.5	
7	R_1	1.94	0.669	0.024	−16.8	
8	R_2 R_3 R_4	2.02	0.698	0.029	−14.8	
9	R_2 R_3	2.11	0.728	0.030	−12.7	
10	R_2 R_4	2.21	0.761	0.033	−10.5	
11	R_2	2.31	0.798	0.037	−7.9	
12	R_3 R_4	2.42	0.834	0.036	−5.4	
13	R_3	2.55	0.881	0.047	−2.2	
14	R_4	2.71	0.936	0.055	+1.6	Max
15	None	2.9	1.0	0.064	+6.0	Volume

The Δ column indicates the difference in the VLC/V_B ratio as the count is increased. The steps are larger at the high volume end compared to the low volume end. It is believed that this is not objectionable in most applications, and in fact, some users consider it desirable. The "dB Gain" column indicates the gain of the receive attenuator derived from Figure 5 of the data sheet.

Situation 2

For the MC34118 with a fixed supply voltage, the value of the resistors will depend on the specific voltage used for V_{CC}. Since the minimum VLC is 0.3 V_B, R_A was raised and the equivalent R_B lowered (from the values of situation 1) to achieve the lower ratio. The values for the five resistors can be found from the following chart:

V_{CC}	V_B	R_A	R_1	R_2	R_3	R_4	Min VLC/V_B
6.5	2.8	39K	15K	30K	62K	120K	0.298
6.0	2.54	43K	15K	30K	62K	120K	0.298
5.5	2.29	47K	15K	30K	62K	120K	0.303
5.0	2.04	56K	15K	30K	62K	120K	0.296
4.5	1.79	39K	7.5K	15K	30K	62K	0.296
4.0	1.54	51K	7.5K	15K	30K	62K	0.301

Testing of the circuit with V_{CC} = 5.0 V yielded the following results:

Q_3–Q_0	VLC	VLC/V_B	Δ	dB Gain
0	0.607	0.296		−33.0
1	0.628	0.306	0.010	−29.4
2	0.643	0.313	0.007	−26.1
3	0.669	0.322	0.009	−23.1
4	0.680	0.332	0.010	−20.1
5	0.712	0.347	0.015	−17.0
6	0.740	0.361	0.014	−14.0
7	0.783	0.375	0.014	−11.0
8	0.796	0.389	0.014	−8.5
9	0.856	0.417	0.028	−5.6
10	0.915	0.446	0.029	−2.9
11	1.01	0.489	0.043	−0.4
12	1.10	0.536	0.047	+1.6
13	1.28	0.624	0.088	+3.6
14	1.52	0.741	0.117	+5.0
15	2.05	1.00	0.259	+5.8

In this case, the fact that the step sizes are smaller at the minimum volume end is particularly advantageous since the MC34118 has a non-linear relationship between the VLC/V_B ratio and the amount of signal attenuation (see Figure 5).

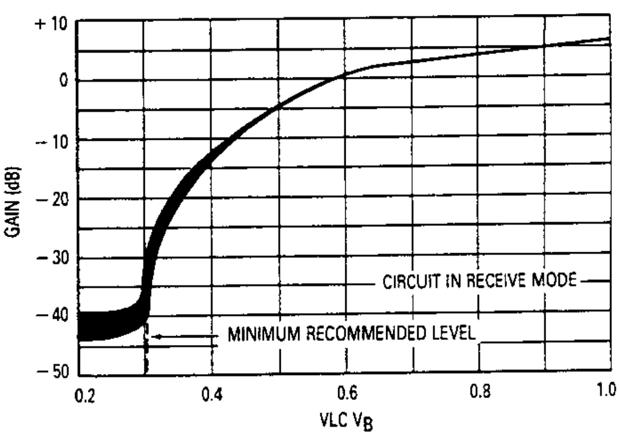

Figure 5. Receive Attenuator versus Volume Control — MC34118

As can be seen from the "dB" column (which is the MC34118's receive attenuator gain setting), the step size, in terms of the dB attenuation, is fairly constant throughout most of the range.

Situation 3

For the case where the MC34118 is used in a line powered speakerphone, V_{CC} can vary from 3.5 to 6.5 V, with a range for V_B of 1.3 to 2.8 V. If the circuit of Figure 4 is used, and set to provide a minimum VLC/V_B ratio of 0.3 when V_B = 2.8 V, the minimum ratio will be considerably higher (≈0.43) when V_B is reduced to 1.3 V. From the graph of Figure 5, it can be seen that the minimum gain will then be −10 dB rather than −33 dB. The problem stems from the ≈0.5 V drop of the diodes, which is a significant part of V_B. To reduce the effects of this voltage drop, the diodes are replaced with NPN transistors which have a saturation voltage of only ≈0.05 V (see Figure 6). The outputs of the MC14516 counter drive the 2N2222A transistors through the 100 kΩ base resistors. Because of the logic inversion of the transistors, the function of the UP and DOWN switches of Figure 3 is reversed. Additionally, because of the inversion, the preset inputs (P_3–P_0) must be changed to 0100 to achieve the same power-up setting as that of Figure 3.

With the circuit of Figure 6, the minimum VLC/V_B ratio ranges from a low of 0.298 (V_{CC} = 6.5 V) to a high 0.312 (V_{CC} = 3.5 V). The tested performance of this circuit, with V_{CC} = 5.0 V, is as follows:

Q_3–Q_0	VLC	VLC/V_B	Δ	dB Gain
0	0.615	0.300		−30
1	0.645	0.314	0.014	−26.5
2	0.674	0.329	0.015	−23.3
3	0.709	0.346	0.017	−20.4
4	0.755	0.368	0.022	−17.4
5	0.800	0.390	0.022	−15.1
6	0.847	0.413	0.023	−13.1
7	0.904	0.441	0.028	−11.1
8	0.970	0.473	0.032	−9.1
9	1.04	0.507	0.034	−7.2
10	1.13	0.551	0.044	−5.4
11	1.24	0.605	0.054	−3.5
12	1.39	0.678	0.073	−1.6
13	1.56	0.761	0.083	+0.7
14	1.77	0.863	0.102	+3.3
15	2.05	1.00	0.137	+5.9

IF YOU HAVE A MICROPROCESSOR . . .

If a microprocessor is included in the speakerphone design, the above circuit can be simplified by letting the processor do the switch de-bouncing, the up/down counting, and the off-hook preset. The critical part of Figure 3's circuit is the resistor network, and it can be controlled from a port through a CMOS latch (see Figure 7).

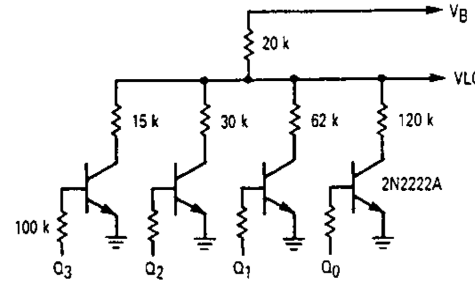

Figure 6. Network for MC34118 Variable Supply Situation

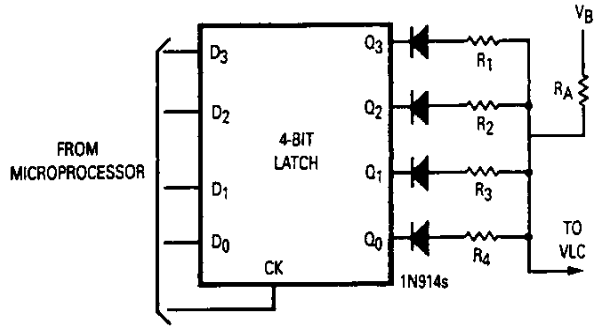

Figure 7. Microprocessor Interface

Recommended latches are the MC14042, MC14076, MC14174, and MC14175. The resistor values depends on which speakerphone circuit is used.

IN SUMMARY . . .

The circuit presented is fairly simple and straightforward without any critical components involved. The accuracy requirements of the resistor network depend on the accuracy requirements of the application. 5% resistors should suffice for most applications. The power supply current required for the additional circuitry is minimal (<1.0 μA) since all CMOS ICs are recommended. Additionally, the wide range of power supply voltages allowed by CMOS devices makes this circuit suitable for use with line-powered speakerphones.

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MC34118 Data Sheet, Motorola, 1987
MC14516 Data Sheet, Motorola
MC14044 Data Sheet, Motorola
MC14001 Data Sheet, Motorola

Literature Distribution Centers:
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